Nearly Unity Power-Factor of the Modular Three-Phase AC to DC Converter with Minimized DC Bus Capacitor

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Abstract—The analysis and design of nearly unity power-factor and fast dynamic response of the modular three-phase ac to dc converter using three single-phase isolated SEPIC rectifier modules with minimized dc bus capacitor is discussed, based on power balance control technique. The averaged small-signal technique is used to obtain the inductor current compensator, thus resulting in the output impedance and audio susceptibility become zero, that is, the output voltage of the converter presented in this paper is independent of the variations of the dc load current and the utility voltage. The proposed system significantly improves the dynamic response of the converter to load steps with minimized dc bus capacitor for Distributed Power System (DPS). A 600 W prototype modular three-phase ac to dc converter comprising three 200 W single-phase SEPIC rectifier modules with the proposed control scheme has been designed and implemented. The proposed system is confirmed by experimental implementation.

Index Terms—Fast response, minimized capacitor, modular rectifier, power factor correction.

I. INTRODUCTION

In recent years, single-phase switch-mode ac to dc power converters have been increasingly used in industrial, commercial, residential, aerospace, electronic equipment and telecommunication systems due to advantages of high efficiency, small size and weight. To improve the power quality, various Power Factor Correction (PFC Boost, Buck, Buck-Boost, SEPIC and CUK) schemes have been proposed [1]. SEPIC and CUK converter presents a current source characteristics, which is suitable for high power factor applications [2]. However, isolated CUK topology is more complex than SEPIC topology. Isolated SEPIC topology utilizes only one switch for controlling power flow, making the drive circuit extremely simple, minimizes line noise and EMI between the input network and the rectifier, operate as step-up or step-down voltage, magnetic coupling and single-stage transformer isolation. Generally, a single high-power power supply has some disadvantage. Therefore, a single-phase parallel configuration using PFC boost [3], SEPIC [4] and CUK topology [5] for dc DPS have been developed. However, a three-phase ac to dc power converter is becoming popular for low voltage or medium power applications [6]. It often require transformer isolation, high power factor, low input current Total Harmonic Distortion (THD), high efficiency and high power density.

Distributed power supply for electronic equipment and telecommunications requires low voltage (-48V), high current as well as very tight transient regulation. This imposes strict requirement for a PFC circuit and step down PWM converters with single-phase or multi-phase. The output capacitors play an important role in the transient response. Many types of capacitors are available in the market such as Aluminum electrolytic, Tantalum, POSCAP, OSCON cap, Specially polymer, as well as large value of multi-layer ceramic capacitors.

In this paper, a nearly unity power-factor and fast dynamic response of the modular three-phase ac to dc converter using three single-phase isolated SEPIC rectifier modules with minimized dc bus capacitor is proposed. The block diagram of the proposed system based on power balance control technique is shown in Fig. 1. This paper shows a control concept to find out the minimum value of capacitors in order to meet the transient requirement. The dynamic behavior of output voltage will be described with different values of output capacitance (Highest case: \(C_2 = 13,600 \mu F\) and Lowest case: \(C_2 = 150 \mu F\)) by experimental results.

![Fig. 1. System configuration block diagram of the modular three-phase ac to dc converter with minimized dc bus capacitor based on power balance control technique.](image-url)
The proposed system is discussed and compared to parallel SEPIC PFC circuit based on power balance control technique. Furthermore, the proposed scheme offers flexibility in either 3-phase 3-wire system or 3-phase 4-wire system, easier testing and higher reliability thanks to the three identical standardized modules. Its main features include: the proposed system is modularity; simple control strategy and design; the second order harmonic current component in the output capacitor is cancelled, this significantly reduces capacitor heating, improves its operating life; a small dc bus capacitor; fast-response load regulation; low THD, and high input power factor. The proposed control strategy for modular three-phase ac to dc converters using SEPIC rectifier modules is useful in those applications requiring the fastest response of the output voltage to load steps.

II. THE PROPOSED SYSTEM

The single-phase isolated SEPIC topology presents a current source characteristic, which is suitable for high power factor applications and it is used to limit the phase interaction problem. The power stage of each power module is a single-phase bridge rectifier and an isolated SEPIC rectifier module. A single dc bus capacitor, C2 is connected at the output terminals for filtering the output voltage ripples. It can be used as dc bus for distributing power to load converter. It is one of the simplest and very interesting for low to medium power application (100-1kW). The power balance control technique for controlling a three-phase ac to dc converter, which is able to handle heavily step load change, module load sharing and power factor correction. It consists of a sinusoidal reference, PI controller and three-inductor current calculators. The inductor current calculator computes the desired ac input phase current. The output voltage is measured and compared to a reference output voltage. The voltage error is injected into an appropriate output voltage controller. The summation signal is multiplied by a signal of each rectified input voltage and then summed. The resulting modulation signal is processed by a suitable hysteresis current control, generating the driving signal to control each switch of that module.

A. System Ratings

In performing the rating analysis, the following assumptions are given. Firstly, All the single-phase isolated SEPIC rectifier module process ideal input current control, i.e., its waveform is purely sinusoidal with unity power factor. Secondly, the source voltage, current, and VA ratings of each single-phase rectifier module are \( V, I \), and \( VI \), respectively. Obviously, \( VI = P_o / \eta \) with \( P_o \) and \( \eta \), respectively, being the output power rating and efficiency of the single-phase rectifier module.

In this case, one can find from Fig. 1 that the rated rms line voltage and current are \( V_L = V \) and \( I_L = \sqrt{3} I \), and the total modular three-phase ac to dc converter rating is

\[
VA_h = P_h = \sqrt{3} V_L I_L = 3 VI
\]

B. Single-Phase SEPIC Rectifier Module

Detailed circuit configuration of single-phase ac to dc converter shown Fig. 1, which consists of a diode full bridge rectifier, a dc to dc isolated SEPIC rectifier module and single output filter. The specifications are given as : source voltage \( V_{in} = 220V \pm 10\% \), line frequency 50 Hz; power factor \( pf \geq 0.95 \); maximum output power \( P_o = 600W \); output DC voltage \( V_o = 48V \); efficiency \( \eta \geq 85\% \). Assume that the SEPIC rectifier modules of the proposed system are operated in CCM, the input current is sinusoidal with unity power factor, and the interaction between modules is neglected. From the specifications given above, one can find: a) the maximum amplitude of the source current \( I_{ij} = \sqrt{3} P_o / (\sqrt{2} V_{in} \min \eta) = \text{1.68 A} \); b) the minimum duty ratio \( d(\omega t)_{\min} = M / (M + n) = 0.23 \), where the diode voltage drops are neglected. By choosing the current ripple in input inductance \( L_{ij} \) to be \( \Delta i_{ij} \leq 0.5A \). The input inductance \( L_{ij} \) is found:

\[
L_{ij} > \frac{\hat{V}_{ij} T_{sw} d(\omega t)_{\min}}{\Delta I_{ij}} = 3.99mH
\]

The measured inductance of the designed input inductor is 5 mH at 30 kHz. The magnetizing inductance \( L_2 \) is found:

\[
L_2 > \frac{\left(\frac{\hat{V}_{ij} d(\omega t)_{\min}}{2 f_{sw} P_o_{\min}}\right)^2}{2 f_{sw} P_o_{\min}} = 768\mu H
\]

The measured magnetizing inductance is 2 mH at 30 kHz. Considering a resonant frequency of 2.5 kHz, the intermediate capacitor is given by

\[
C_1 = \frac{1}{\omega^2 \left(L_{ij} + L_2 \right)} = 0.85\mu F
\]

Pick \( C_1 = 1 \) \( \mu F \).

The output dc capacitance \( C_2 \) is determined according to the hold-up time \( \Delta t_h \) [7]. By choosing \( \Delta t_h \geq 2ms \), one can find

\[
C_2 \geq \frac{2 P_o \Delta t_h}{V_o^2 - P_o^2_{\min}} = 10,683\mu F
\]

Pick \( C_2 = 13,600 \) \( \mu F \).
III. DESCRIPTION OF POWER BALANCE CONTROL APPLIED TO MODULAR THREE-PHASE AC TO DC CONVERTER

The average small-signal analysis of the proposed system is based on a power balance control technique. The model of the proposed system is:

$$\sum_{ij=ab}^c V_{gij} I_{ij} = V_o I_o$$  (6)

When, $ij = ab, bc$ and $ca$, $V_{gij}$ is rectifier voltage, $I_{ij}$ is inductor current, $V_o$ is dc output voltage, $I_o$ is average output current over a half-line cycle. The peak value of the inductor current is

$$\hat{I}_{gij} = \frac{K_2 V_o I_{load}}{3 V_{gij}}$$  (7)

$$\hat{I}_{Refij} = \hat{I}_{ij} + I_{VR}$$  (8)

$\hat{I}_{Refij}$ is peak value of the inductor reference current, $\hat{I}_{ij}$ is peak value of the inductor current, $I_{VR}$ is correcting signal of PI controller, $K_2$ is conversion gain. The dynamic equation of the output voltage is

$$\sum_{i=1}^3 I_o = C_2 \frac{dV_o}{dt} + I_{load}$$  (9)

Where the $\bar{V}$ means steady-state value and $\bar{v}$ means the introduced perturbation. Applying the perturbations in (6), (7), (8), and (9), and performing the small-signal approximation ($\bar{v} = 0$) results in:

$$\hat{v}_o = \frac{3K_1}{V_o} \bar{v}_{Refij} \bar{g}_{ij} + \frac{3K_2}{V_o} \bar{g}_{ij} \hat{I}_{Refij} - \frac{T_o}{V_o} \bar{v}_o$$  (10)

$$\hat{I}_{Refij} = \hat{I}_{ij} + I_{VR}$$  (12)

$$\bar{I}_{ij} = \frac{K_2 \bar{v}_o}{3 V_{gij}} I_{load} + \frac{K_2}{3 V_{gij}} \bar{v}_o - \frac{K_2^2 T_{load}}{3 \bar{V}_{gij}} \bar{v}_{gij}$$  (13)

The transfer function of the proposed system is:

$$\frac{\bar{v}_o}{\bar{v}_{Refij}} = \frac{3G_{VR} \bar{V}_{gij} K_1}{V_o C_2 S + 3G_{VR} \bar{V}_{gij} K_2 k_{fb}}$$  (14)

Generally, the goal is simply a bode plot constructed to achieve the best system dynamic response, tightest line and load regulation, and greatest stability. According to Nyquist’s stability criterion, a system is stable when its phase margin exceeds 0°. However, a region of marginal stability exists where the system transient response oscillates and eventually damps out after a long settling time. A system is marginally stable if it phase margin is more than 45° provides the best dynamic response, short settling time and minimal amount of overshoot. Applying classical control loop analysis techniques, the control loop of the proposed system is divided into three main stages, gain of the proposed system and output filter, error amplifier compensation, and feedback gain.

Feedback transfer function is:

$$k_{fb} = \frac{R_2}{R_1 + R_2}$$  (15)

Here, a PI controller is chosen for voltage regulation

$$G_{VR}(s) = k_p \left(S + s \omega_Z\right) S$$  (16)

Plant Transfer Function is:

$$PTF(s) = \frac{3 \bar{V}_{gij} K_1 k_{fb}}{V_o C_2 S}$$  (17)

Open Loop Transfer Function is:

$$OLTF(s) = \frac{3G_{VR}(s) \bar{V}_{gij} K_1 k_{fb}}{V_o C_2 S}$$  (18)

Table 1 shows the design results of a 600W, 48V, three-phase ac to dc using isolated SEPIC rectifier modules. The frequency response analysis is used to describe the stability of the proposed system [8]. The design of the output voltage control loop must guarantee the stability and enough bandwidth in all the possible operation conditions of the proposed system. A suitable network is based on integral action (zero and high frequency).

<table>
<thead>
<tr>
<th>Table I</th>
<th>SPECIFICATION AND PARAMETERS OF THE PROPOSED SYSTEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Characteristic</td>
<td>SEPIC rectifier modules</td>
</tr>
<tr>
<td>Input voltage ($V_{in}$, $V_{in}$)</td>
<td>220 V</td>
</tr>
<tr>
<td>Line frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Rated Module</td>
<td>200 W/module</td>
</tr>
<tr>
<td>Total output power</td>
<td>600 W</td>
</tr>
<tr>
<td>Output voltage</td>
<td>48 V</td>
</tr>
<tr>
<td>$L_{11}$, $L_{21}$</td>
<td>5.089 mH, 2.142 mH</td>
</tr>
<tr>
<td>$L_{12}$, $L_{22}$</td>
<td>5.047 mH, 2.151 mH</td>
</tr>
<tr>
<td>$L_{13}$, $L_{23}$</td>
<td>5.006 mH, 2.161 mH</td>
</tr>
<tr>
<td>$C_{11}$, $C_{12}$, $C_{13}$</td>
<td>1 µF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>13,600 µF (max), 150 µF (min)</td>
</tr>
<tr>
<td>$n$</td>
<td>0.5</td>
</tr>
<tr>
<td>$k_{fb}$, $\omega_Z$</td>
<td>1, 150</td>
</tr>
</tbody>
</table>
With balance three-phase operation, there is no low-frequency ripple in the output voltage. Hence, the output voltage control loop can be designed for higher or lower bandwidth, resulting in dynamic response. The Bode diagram of (16), (17) and (18) is presented in Fig. 2. Since this is a linear system, superposition technique can be applied to drive the overall system transfer function. By superimposing the gains and phases of the stage around the loop, a Bode plot of the overall system is generated. The high-frequency gain and zero of the compensation network can then be placed to optimize the system performance. Fig. 2 combines the Bode plots of the stages and 180° phase shift is also added to account for the negative feedback of the system. The voltage loop is designed to have a crossover frequency of 60 Hz. It also gives a 67.5° phase margin.

IV. EXPERIMENTAL RESULTS

A. Parallel Single-Phase SEPIC PFC Circuit

The analysis and design of a parallel SEPIC PFC circuit based on power balance control technique has been analyzed in Reference [9]. Transient response condition of parallel single-phase configuration, when N=3 are shown in Fig. 3. Fig. 3(a) shows the waveform of source voltage and current at power output step change from 600W(100%) to 300W(50%). Fig. 3(b) shows the closed up of individual inductor current while load has been changed from 600W to 300W. Fig. 3(c) shows the transient response of output voltage at 48V (ΔV_o=6.66%, C_2= 13,600 μF) and load current at 12.5A. Since, the single-phase parallel SEPIC PFC circuit results in large ripple in the output voltage, frequency is a twice of the line frequency to be 100Hz. The input current is significantly distorted when the output voltage ripple is large. Although very large output filtering capacitors can be used to reduce the output voltage ripple and thus results in better input current waveform, the drawbacks are their bulky size, high prices and capacitor heating. The concept of power balance control technique will be extended to evaluate the dynamic performance and minimized output capacitance of the three-phase ac to dc converter using SEPIC rectifier modules.

B. Modular Three-Phase ac to dc Converter with Power Balance Control Technique and Its Behavior

The experimental results from a 600W, 48V three-phase ac to dc converter using three isolated single-phase SEPIC rectifier modules based on power balance control technique are shown through Fig. 4 to Fig. 11. A simple PI controller is used for the output voltage control loop. Three-inductor current calculator feeds the current references of the three single-phase rectifier modules forcing current sharing between them. The effectiveness of the power balance control technique is examined by analog circuitry. The objective is to find the limits of the dynamic characteristics of these proposed system when priority is to improve the output voltage regulation,
minimized dc output capacitor with low total harmonic distortion and high input power-factor. A 600W prototype modular three-phase ac to dc converter comprising three 200W single-phase isolated SEPIC rectifier modules has been designed and built. Each converter operates in continuous conduction mode (CCM) together with hysteresis current control. Fig. 4 shows the experimental results of the dc bus voltage to a load step from 10% to 100% with and without the power balance control technique. The upper trace of Fig. 4(a) is the dc bus voltage and the lower one is the load current during transient. Its can be seen that the output voltage waveform has a large dip and a longer settling time, indicating a poor dynamic performance. Fig.4 (b) shows that, during the transient, the output voltage waveform recovery quickly without voltage dip, indicate very good dynamic performance. The settling time of the transients without power balance control technique is 30 ms and the one with power balance control technique is about 100 μs. These results demonstrate that even without power balance control technique, the dc bus voltage response is effected by load variation. Steady state condition of the proposed system with two different values of dc bus capacitor (C_{2min}=150 μF, and C_{2max}=13,600 μF) at rated input and output voltage and output power (220V, 48V and 600W). They are measured with the Digital power meter YOKOKAWA model 2531A. The following can be concluded
1. Power factor at rated load is nearly unity, greater than 0.99 for all difference values of output capacitor.
2. Input current THD remains low, lower than 4% at rated load (600W), for twenty-one values of output capacitor.

Thus, the input power factor approaches unity. They have been illustrated that the proposed system can achieved a high power factor. Due to the effects of difference inductance values and parasitic in input inductors, these three input currents are not exactly equal. However, all input current has approximately same amplitude.

C. Performance Evaluation

The main performance features of the proposed system for input power-factor and input current total harmonic distortion (THDi) are plotted in Fig.6 as a function of the different DC capacitor size (C_{2max}=13,600μF, and C_{2min}=150μF) at rated input and output voltage and output power (220V, 48V and 600W). They are measured with the Digital power meter YOKOKAWA model 2531A. The following can be concluded
1. Power factor at rated load is nearly unity, greater than 0.99 for all difference values of output capacitor.
2. Input current THD remains low, lower than 4% at rated load (600W), for twenty-one values of output capacitor.

The transient operation of the modular three-phase ac to dc converter depends to a large extent on the dc bus capacitor. The influence of its value on ΔV_{droop}, ΔV_{overshoot} and settling time is shown in Fig. 7. The
voltage droop or overshoot is typically unsymmetrical. As expected the settling time decreases as the capacitance increases, down to 100 µs for C₂ ≥ 3,000 µF, and the ΔV_{droop}, ΔV_{overshoot} decreases as well. The voltage ΔV_{droop} is higher than ΔV_{overshoot} for C₂ < 1,000 µF. At low values of dc bus capacitor with C₂ < 470µF, the total ΔV_{droop} and ΔV_{overshoot} is larger than 5% and Δt of the settling time is very large. However, for high values of dc bus capacitor with 3,000 µF ≤ C₂ ≤ 13,600µF, the voltage droop and overshoot is nearly zero and Δt of the settling time is nearly zero as well.

D. Investigated Range Based on Step Transient Response

Generally, the voltage droop and overshoot specification during the transient is very tight and it is typically ±5% of nominal output voltage [10]. In order to meet the transient requirement, the selection of dc bus capacitors is very critical. This section deals with this tradeoff between output capacitance and output voltage regulation for the dynamic limits of the proposed system. The experimental results of the proposed system operating at step load change from 60W to 600W under six different output capacitors (150µF, 270µF, 330µF, 470µF, 820µF and 1,000µF) are shown in Fig. 8(a) to 8(f), respectively. The comparison between the results indicates that the small voltage dips and less variant in response trajectories are yielded by applying power balance control technique.

Fig. 6. Performance as a function of dc capacitor size. (Power factor, Source current THD, V_S=220V, V_O=48V and P_D=600W).

Fig. 7. Performance as a function of dc capacitor size under condition step load change from 600W(100%) to 60W(10%) and vice versa. (V_S=220V and V_O=48V).

Fig.8. Experimental results of dc bus voltage (V_O : 10V / div) and load current (I_{load} : 5A / div, Time : 400µs / div) at step load change from 10%(60W) to 100%(600W) parameter of PI controller K_p=1 and T_Z=150).
If we define optimal range of dc bus capacitor is $C_{2\text{optR}}$. The physical meaning of $C_{2\text{optR}}$ is how fast the system recovers during the transient. The $\%\Delta V_{o} \leq \%\Delta V_{\text{target}}$ (5%) is, the system recovers faster. For the optimal range of dc bus capacitor with 470$\mu$F, the total ($\%\Delta V_{\text{group}}$ and ($\%\Delta V_{\text{overshoot}}$ is lower than 5% and $\Delta t$ of the settling time is very small ($\approx 30\mu$s). From this point of view, it is desirable to have as fast output voltage loop response as possible if the optimal dc bus capacitor is employed.

V DISCUSSIONS

Table II shows the transient performance indexes at investigated range of dc bus capacitor. It can be observed that the settling time, percentage output undershoot and overshoot decreases, as the dc bus capacitor increases. Although the optimal value of output capacitor is chosen, the compromise between control performance and output capacitor should be considered. Thus, $C_{2}=470\mu$F is adopted in the power circuit component. Steady state and transient response conditions of the proposed system with minimized dc bus output capacitor are shown in Fig. 9(a) to 9(f), respectively. Figure 9(a) shows input voltage and three-input current waveforms of the proposed system. Three input currents are in phase with their relative input voltages and nearly sinusoidal. Thus, the input power factor approaches unity. They have been illustrated that the proposed system can achieve a high power factor. Figure 9(b) and 9(c) shows three-phase input currents and three-inductor currents at full load. Due to the effects of difference inductance values and parasitic in input inductors, these three input currents and three-individual inductor current are not exactly equal. However, all input and inductor current has approximately same amplitude. Figure 9(d) shows the dynamic response of the output voltage and load current of the proposed system due to step load changes at the load current between 100% to 10% and vice versa. Figure 9(e) and Fig. 9(f) shows closed up of transient response condition due to step load changes at 100% to 10% and 10% to 100%, respectively. The voltage droop or overshoot is typically unsymmetrical. The voltage droop and overshoot are 3.12% and 1.04%, respectively. The settling time is 430 $\mu$s. It can be seen that such scheme is effective and fast transient response characteristic. The performance measurements of the modular three-phase ac to dc converter with minimized dc bus capacitor are reported, in terms of input power factor, input current THD, efficiency and harmonic current comparing with the standard IEC 61000-3-2 class A limits. Fig. 10 shows the current harmonics of the proposed system versus load variations. It shows the magnitude of the measured input current harmonics for the three-phase system operating under different power levels. It meets the regulation of IEC 61000-3-2 Class A limits. Fig. 11 shows the key performance of the proposed system at different output power.

<table>
<thead>
<tr>
<th>$C_{2}$ ($\mu$F)</th>
<th>Setting time ($\mu$s)</th>
<th>% output undershoot</th>
<th>% output overshoot</th>
<th>Max. load current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150$\mu$F</td>
<td>1,200</td>
<td>8.33</td>
<td>6.25</td>
<td>12.5</td>
</tr>
<tr>
<td>270$\mu$F</td>
<td>800</td>
<td>6.25</td>
<td>4.16</td>
<td>12.5</td>
</tr>
<tr>
<td>330$\mu$F</td>
<td>520</td>
<td>4.16</td>
<td>2.08</td>
<td>12.5</td>
</tr>
<tr>
<td>470$\mu$F</td>
<td>430</td>
<td>3.12</td>
<td>1.04</td>
<td>12.5</td>
</tr>
<tr>
<td>820$\mu$F</td>
<td>400</td>
<td>2.08</td>
<td>1.04</td>
<td>12.5</td>
</tr>
<tr>
<td>1,000$\mu$F</td>
<td>400</td>
<td>1.04</td>
<td>1.04</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Fig. 9. Experimental results of the modular three-phase ac to dc converter with minimized dc output capacitor ($C_{2}=470\mu$F).
The upper curve in Fig.11 presents the measured power factor for different output power. For the rated load condition the input power factor is high, greater than 0.99, the overall efficiency remains high, approximately 90%, and THD less than 4% at maximum load. In this case, dc bus capacitor \( C_2 = 470 \mu F \), the DC output voltage is regulated to have good transient responses by the designed PI controller with power balance control technique. It should be noted that this dynamic response is fast enough for many conventional industrial applications and hence, no second stage is needed. Thus, the proposed regulator is relatively feasible in medium-power applications, which has been verified by the measured results.

VI. CONCLUSIONS

The paper has demonstrated that, with a minimized DC bus capacitor and power balance control technique, excellent power factor correction, module load sharing under load transitions and high overall efficiency can be achieved for a modular three-phase ac to dc converter using three single-phase isolated SEPIC rectifier modules. Control circuit is simple and can be implemented by analog circuit. The experimental results prove that proposed system are improved the transient response with minimized DC bus capacitor. Also, the proposed system is meet harmonic distortion standards and requirements (IEC61000-3-2 Class A limits).

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