Resolver-signal Demodulator Using Phase Shifter
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Abstract

An alternative approach to implement the fast resolver-signal demodulator is presented in this paper. The realization technique is utilized the phase shift behavior of all-pass filter connected with designed logic circuit to generate the reference signal from exciting signal of resolver rotor. The proposed demodulator produces two output signal voltages, which are proportional to sine and cosine envelopes of resolver-shaft angle without low-pass filter circuit. Experimental results verifying the performance of the proposed circuit are closely agreed with the expected values.

Keywords: Resolver-signal, demodulator, resolver converter, all-pass filter, phase shifter.

1. Introduction

Resolver is rugged and reliable transducer for measuring speed and angle of rotary devices. It is used in the form of various positioning applications such as robots, aircrafts, and satellite tracking antennas [1-3]. Usually, the resolver outputs (sine and cosine signals) are the analog amplitude-modulated signal in double side-band suppressed carrier (DSB-SC). To achieve a signal linearly proportional to shaft-angle, demodulator followed by the digitization enabling determination of the angle from sine and cosine signals could be employed. One of well known demodulators is implemented with an analog multiplier and a low-pass filter circuit [1]. However, this approach consists of phase lag due to R-C network used in circuit. The second approach is implemented by using two sample-and-hold circuits triggered by pulses occurring at the peaks of resolver-signals. The pulses are conveniently derived from the square wave output of the function generator by using R-C differentiator circuit [2]. An alternative method using JK-flip-flop-based control signal generator for control peak detector followed by sample-and-hold circuit, and ±unity-gain amplifier in sequential operation is introduced in [3]. This technique utilizes peak detector characteristic to holding the peak amplitude of the resolver-signal before sample-and-hold circuit action. However, the detection time requires two cycle time-periods of the input signal used. In order to enhance the operation speed, this paper aims to present a new control signal generator for resolver-signal demodulator, which requires only one cycle time-period of input signal.

2. Circuit Descriptions

Fig. 1(a) shows the amplitude detector for resolver-signal $V_s$ controlled by all-pass filter-based (or phase-shift-based) control signal generator. When the input signal of all-pass filter is the excitation signal $V_{ex}$ of the resolver. Two possible waveforms of the $V_s$ are corresponding to the $V_{ex}$; in phase and out of phase (180-degree inverting). To prevent error of sequential operation during negative envelope (out of phase case), the full-wave rectifier is then used to rectify the signal $V_s$. The waveform sketches relating to various nodes are shown in Fig. 1(b). The sequential operation of the detector circuit can be divided into four steps, which are similar to the method in literature [3]. Firstly, the peak amplitude $K_1$ of $V_s$ is tracking and holding. Secondly, the $K_1$ is sampled and sent into the output signal $V_A$. Next, the last value of $K_1$ is held until the next sample period. Lastly, the output voltage of the peak detector is reset for succeeding tracking. All steps are operated with in one cycle time-period of the input signal. Therefore, the operation of the proposed circuit is faster than that of the scheme reported in [3]. The all-pass filter formed by current conveyor (CCII) in Fig.1 provides the relation of phase shifted-signal $V_{all}$ to the of the signal $V_{ex}$, which can be written as

$$H(s) = \frac{V_{all}}{V_{ex}} = \frac{1 - sC_{al}R_{al}}{1 + sC_{al}R_{al}}$$  \hspace{1cm} (1a)

$$|H(s)| = 1$$ \hspace{1cm} (1b)

$$\angle H(s) = -2 \arctan \omega C_{al}R_{al}$$ \hspace{1cm} (1c)

where $V_{ex}$=$A_{ex}$ sin $(2\pi f_{ex}t)$ and $s=j\omega = j2\pi f_{ex}$
The signals $V_{ex}$ and $V_{al}$ are converted into square-wave signals $Q_{c1}$ and $Q_{c2}$, respectively. Each square-wave signal is applied to the logic circuit for providing the control signals ($Q_{peak}$ and $Q_{sh}$). From waveform sketches in Fig. 1(b), suitable conditions are used to generate signals $Q_{sh}$ and $Q_{peak}$ corresponding of $V_{ex}$ in phase-range $\pi/2-\pi$ and $3\pi/2-2\pi$, respectively. Fig. 2 shows the simulated frequency responses of the all-pass filter circuit by using parameters $C_{al1} = 0.1 \mu F$ and $R_{al} = 1.599 k\Omega$. The proposed demodulator allows the frequency of signal $V_{ex}$ to be varied in range of 1 kHz to 20 kHz.

To verify the performance of the basic principle of amplitude detector, the circuit in Fig. 1(a) were experimentally tested by setting two different frequencies of signal $V_{ex}$: 1 kHz and 10 kHz. The measured signals are shown in Fig. 3(a) and 3(b). It can be seen that the detector in Fig. 1(a) functions correctly.
Based on Fig. 1(a), the proposed demodulator for use with the resolver is illustrated in Fig. 3. Fig. 4 shows waveform sketches relating various nodes of the proposed circuit. It is seen that the peak amplitude of input $V_s$ can be tracked by using the proposed demodulator.

Fig. 3 Proposed resolver-signal demodulator.

Fig. 4 Waveform signals of the proposed circuit.
3. Experimental Results

To verify the performances of the proposed demodulator, the circuit as shown in Fig. 3 was implemented on the breadboard using commercially available devices. A synchro resolver (Sanyo Denki, 101-4100) driven by variable speed dc motor was used as an illustrative case study. The frequency of the excitation signal is set to 3 kHz. Comparators Comp.1-Comp.4 were constructed by using LM319 ICs. The CMOS-gate components were selected for all logic gates. The OP07, D1N4148, CD4066BC, and AD844 devices were used for op-amps, diode, analog-switches and CCII, respectively.

Fig. 5 shows measured resulting signals of various nodes in the circuit of Fig. 3. It is evident that all measured signals are agreed well with the expected signals shown in Fig. 4.

Fig. 5 Experimental results of the proposed circuit.

4. Conclusion

The realization technique based on the phase shift behavior of all-pass filter to enhance the operation speed of the demodulator for resolver has been described in this paper. The proposed demodulator can produce two output signal voltages, proportional to sine and cosine envelopes of resolver-shaft angle, without low-pass filter. Experimental results agreed well with the expected values confirm that the proposed circuit actions correctly.

References

