

การออกแบบและสร้างวงจรกรองสัญญาณเชิงเลขคณิตผลตอบสนองอิมพัลส์จำกัดด้วยอุปกรณ์ FPGA
DESIGN AND IMPLEMENTATION OF FIR DIGITAL FILTER USING FPGA

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บทคัดย่อ: บทความนี้นำเสนอการออกแบบวงจรกรองสัญญาณเชิงเลขคณิตผลตอบสนองอิมพัลส์จำกัด โดยขั้นตอนการออกแบบเพื่อหาผลตอบสนองอิมพัลส์และจำลองการทำงานของวงจรจะใช้โปรแกรม Matlab ช่วยในการออกแบบ ส่วนในแง่การสร้างเป็นฮาร์ดแวร์ เมื่อได้ค่าผลตอบสนองอิมพัลส์แล้วจะทำการจัดโครงสร้างโดยใช้โครงสร้างแบบเฟสเชิงเส้น ซึ่งอาศัยคุณสมบัติสมมาตรของผลตอบสนองอิมพัลส์เพื่อลดตัวคูณลง จากนั้นจะทำการบรรยายพฤติกรรมการทำงานของวงจรกรองสัญญาณที่ได้ด้วยภาษา VHDL แล้วทำการสังเคราะห์รวมทั้งเม็ปวงจรถ่ายไปยังอุปกรณ์ FPGA สำหรับทดสอบการทำงานเทียบกับผลทางทฤษฎี

Abstract: This paper presents a design of Finite Impulse Response (FIR) Digital Filter, these impulse responses can be designed and simulation results can be shown by Matlab program. The hardware implementation can be realized using linear phase structure, symmetrical property of impulse responses will be considered to reduce number of multipliers. Finally an implementation can be used VHDL (Very high speed integrated circuits Hardware Description Language) to describe the hardware of FIR digital filter and synthesis for mapping on FPGA (Field Programmable Gate Array) for testing all results compared with theoretical results.

Methodology: For FIR digital filter can be used impulse responses $h(n)$ for hardware realization. The operation of digital filter is convolution between $h(n)$ with input signal $x(n)$ as shown in figure 1.

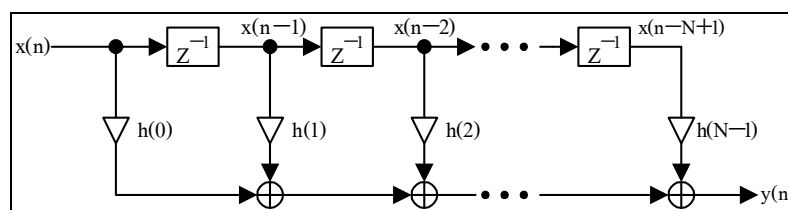


Figure 1. Direct Form FIR Structure

Convolution between $h(n)$ with $x(n)$ defined by

$$y(n) = x(n) * h(n) = \sum_{i=0}^{N-1} h(i)x(n-i) \quad (1)$$

Normally the number of multipliers will decrease the speed of digital filter since the multiplying stage consume process and use large area in design. Therefore, using symmetrical property of impulse responses. Also the difference equation for 16 orders can be rewritten from equation (1) to equation (2) and result in multipliers reduction by half when compared with direct form.

$$\begin{aligned}
 y(n) = & h(0)[x(n) + x(n-15)] + h(1)[x(n-1) + x(n-14)] + h(2)[x(n-2) + x(n-13)] \\
 & + h(3)[x(n-3) + x(n-12)] + h(4)[x(n-4) + x(n-11)] + h(5)[x(n-5) + x(n-10)] \\
 & + h(6)[x(n-6) + x(n-9)] + h(7)[x(n-7) + x(n-8)]
 \end{aligned}
 \tag{2}$$

From equation (2) can be shown linear phase structure in figure (2).

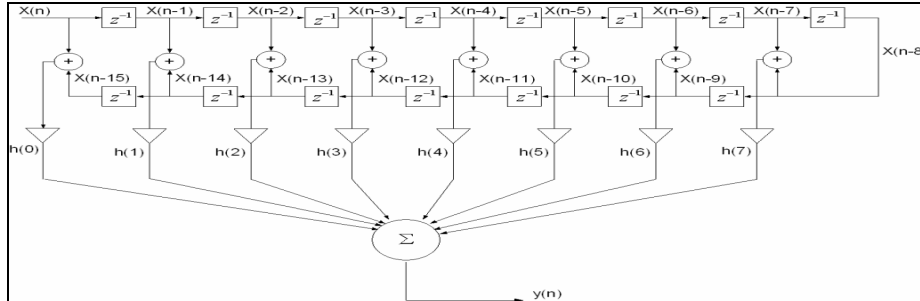


Figure 2. Linear Phase FIR Structure

In experiment will be used FIR lowpass filter 16 orders for testing. The impulse responses of designed filter can be obtained from Matlab which have specifications as follows, sampling frequency 100 kHz, cutoff frequency 5 kHz, number of bits for representation in binary format 12 bits. Since using VHDL for describe the behavior of hardware and synthesis to circuits for implement on EPF10K20RC240-4 Altera FPGA.

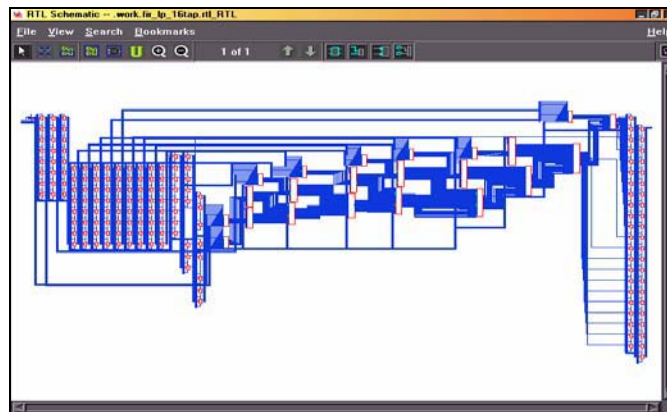


Figure 3. Synthesis Result of Circuits in RTL (Register Transfer Level)

Experimental test set can be shown in figure 4.

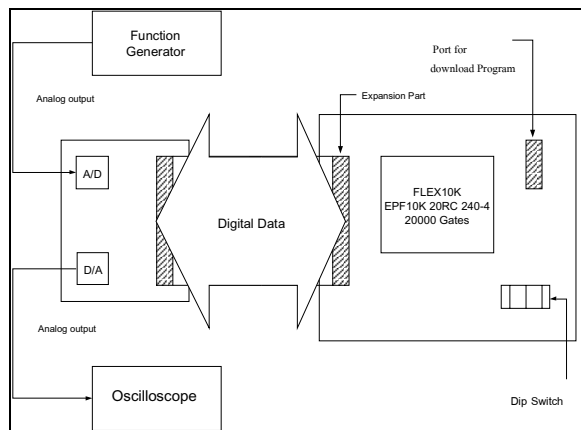


Figure 4. Experimental Test Set

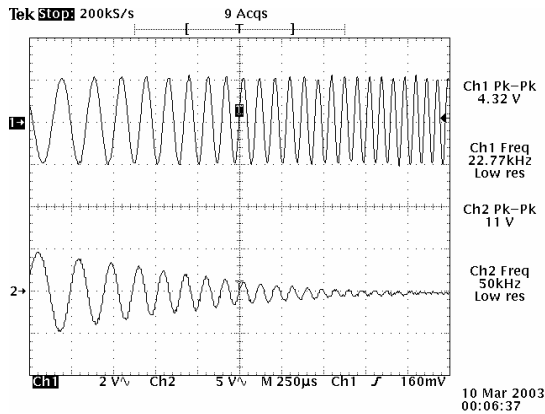


Figure 5. Result from frequency sweeping

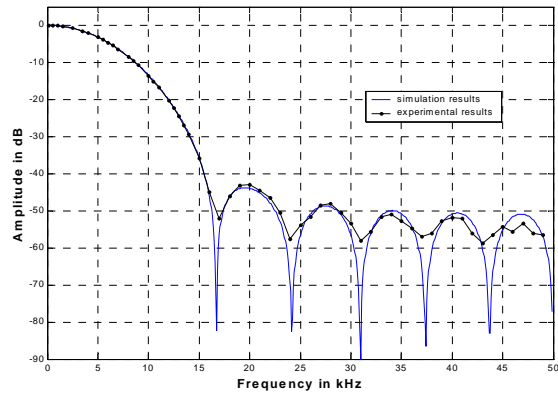


Figure 6. Frequency Response

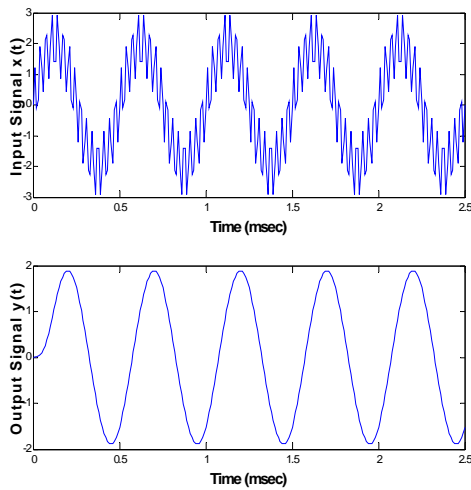


Figure 7. Simulation Result

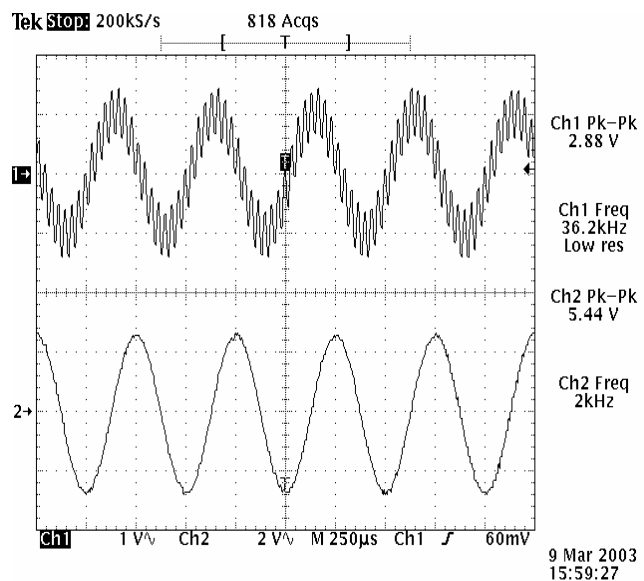


Figure 8. Experimental Result

Results, Discussion and Conclusion: In experiment, can see that the operation performs as lowpass filter by sweeping the input frequency as shown in figure 5. Figure 6. shows the frequency response of designed filter which can see that same as theoretical result. Finally, adding high frequency component to baseband frequency for real world testing compared with simulation result as shown in figure 7. and figure 8. Consequently, from all results FPGA become FIR digital filter and can be developed to mass production integrated circuits because the method for FPGA design similar to digital integrated circuits design.

- References:** (1) Iferchar, E.C. and Jervis, B.W.(1993) Digital Signal Processing A Practical Approach, Addison_ Wesley.
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Keywords: Digital Filter, FPGA, VHDL