A Three-Phase Space-Vector Based PWM Rectifier with Power Factor Control

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***Abstract*—A three-phase space-vector based PWM rectifier with power factor control has been proposed in this paper. The three-phase phase locked loop (PLL) is designed to detect the phase angle of utility voltage, which is used to create three-phase reference currents. The proposed scheme is simple and practical to be implemented on a fixed-point digital signal process based controller. It also does not require any system parameters. According to experimental results, the dc output voltage is successfully controlled while the unity power factor is accomplished.**

***Index Terms*—phase locked loop, power factor control, rectifier, space-vector PWM, unity power factor.**

I. INTRODUCTION

According to the international standards such as IEC1000-3-2, EN61000-3-2, and IEEE519, the modern rectifiers are required to limit the current harmonics and to implement the power factor correction. In literatures, several algorithms of three-phase PWM rectifier have been proposed to accomplish such requirements. In [1], the modified hysteresis current control was proposed to reduce the current ripples and the number of switchings per cycle, comparing with the conventional hysteresis current control. However, this modified hysteresis current control may require the fast A/D conversion and high-frequency digital controller when it is implemented digitally. Secondly, the one-cycle current control technique was proposed in [2]. Although the technique is simple to implement, the duty cycles of switches are directly calculated based on the measured currents in the open-loop fashion. Thus, the sensitivity of control strategy is highly dependent to the quality of current measurement, comparing with other current closed loop techniques. In [3], the overall power factor control system implements the instantaneous active and reactive power controls rather than the current controls (so called direct power control). The powers are computed by using the virtual estimated flux and line currents. However, this virtual flux estimator ignores the line resistor and requires the precise value of line inductor. In [4], the repetitive current controller was designed to take care of the parameter uncertainties used in the deadbeat controller (fast one-sampling controller). However, most parameters are still necessary to be known in order to check the system stability. This paper presents the dq-axis current closed loop controls based on space-vector PWM [3,5], providing a constant switching frequency operation (predictable switching losses). The ISR control loop and A/D sampling frequencies are not necessarily high as well (slow fixed-point DSP based controller is possible). Unlike other schemes, the proposed algorithm does not require any system parameters, so it is obviously insensitive to the parameter inaccuracies.

II. PRINCIPLE OF THREE-PHASE SPACE-VECTOR BASED PWM RECIFIER WITH POWER FACTOR CONTROL

A. Three-Phase PLL

The phase angle of utility voltages is very important variable for implementing the power factor control. Since the reference sinusoidal currents are created by using this angle. In this section, a three-phase PLL scheme is explained. Figure 1 shows its structure when line-line voltages are measured in the system as the PLL inputs. This structure is based on the synchronism between the utility line-line voltage angle (θ_L) and computed angle of synchronously rotating reference frame (θ_{comp}).

In Fig. 1, the Clarke and Park transformations with θ_{comp}, are used to compute the dq-axis line-line voltages, which are shown below

$$\begin{aligned} E_{ds} &= E_p \cos\theta_L \cos\theta_{comp} + E_p \sin\theta_L \sin\theta_{comp} \\ &= E_p \cos\left(\theta_L - \theta_{comp}\right) \end{aligned} \quad (1)$$

$$\begin{aligned} E_{qs} &= E_p \sin\theta_L \cos\theta_{comp} - E_p \cos\theta_L \sin\theta_{comp} \\ &= E_p \sin\left(\theta_L - \theta_{comp}\right) \end{aligned} \quad (2)$$

where the measured line-line voltages are expressed as

$$\begin{aligned} E_{ab} &= E_p \cos\theta_L \\ E_{bc} &= E_p \cos\left(\theta_L - 2\pi/3\right) \end{aligned} \quad (3)$$

As seen in (2), when the E_{qs} is controlled to zero by PI controller, then the PLL angle, θ_{comp}, eventually becomes the angle of line-line voltages, θ_L. In addition to that, the E_{ds} also becomes the peak of line-line voltages, E_p. The PLL angle θ_{comp} is simply computed by an integrator of two frequencies, i.e., the known line frequency (ω_{ff}) and PI output (U). The PI output is merely the frequency that is adjusted in such a way that E_{qs} approaches to zero,

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resulting in the θ_{comp} be matching with the θ_L. In this case, the angle of phase voltages is wanted instead of the angle of line-line voltages, thus the additional angle $\theta_{offset} = -30^\circ$ is finally added.

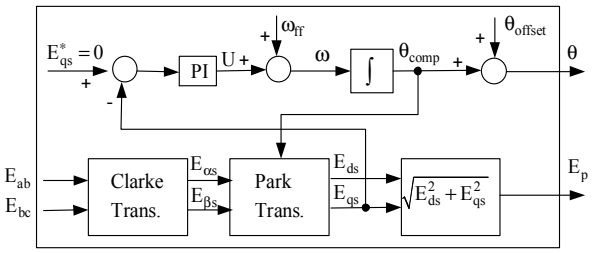


Fig. 1. Structure of three-phase PLL.

B. *Three-Phase Space-Vector Based PWM Rectifier*

Figure 2 shows the topology of the typical three-phase PWM rectifier circuit containing three line inductors (L_a, L_b, and L_c). In this circuit topology, the boost operation is possible when the switching devices are properly operated. There are six switching regions, which are determined by the angle of phase input voltages (E_a, E_b, and E_c) as shown in Fig. 3. The upper and lower switches in each phase are always operated complementary. Switches of two phases are driven by PWM mode while ones of another phase are always turned on or off during each region. Table 1 summarizes the switching schemes and the available voltage vectors in each region. The voltage space vector diagram and the switching logics of upper switches (Q1,Q3,Q5) for each voltage vector can be seen in Fig. 4.

When using the switching schemes in table 1, the dc output voltage (V_o) can be boost up in each region. Figure 5 depicts the equivalent circuits associated in each region and Table 2 summarizes their circuit parameters. These circuits are actually the parallel-connected dual boost converter. For example, in the first region when ac input voltages (E_{ab} and E_{cb}) are always positive, the duty cycles of switches Q6 and Q2 are controlled such that the desired V_o is met. During this region, the switch Q4 is always turned on, so the voltage vectors V_5, V_6, V_1, and V_8 are available to control the V_o. In addition to the dc output voltage control, the line currents (I_a, I_b, and I_c) are also shaped in phase with the phase voltages (E_a, E_b, and E_c). The overall system of 3-ph PWM rectifier with PFC can be illustrated in Fig. 6. The output of PI output voltage controller gives the proper peak of reference currents, reflecting the output power. Three-phase abc-axis currents are transformed to synchronously rotating dq-axis currents by using Park transformation. Then, two PI current controllers control these constant dq-axis currents. The outputs of these controllers give the required dq-axis voltages applying to the rectifier. Finally, the space-vector PWM technique is used to operate the switches.

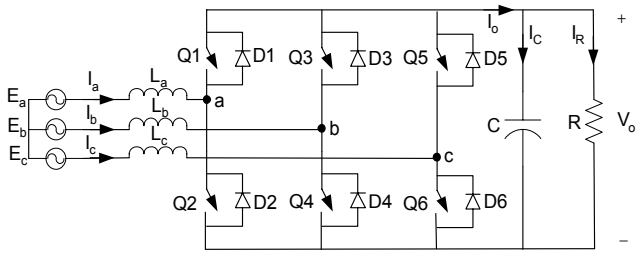


Fig. 2. Three-phase PWM rectifier with PFC.

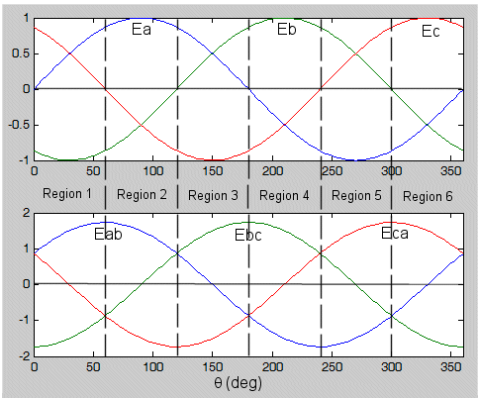


Fig. 3. Six switching regions.

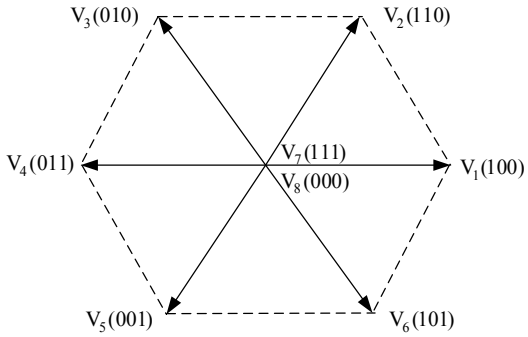


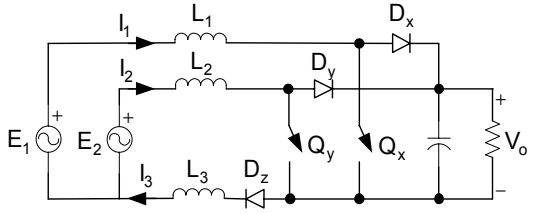
Fig. 4. Voltage space vector diagram.

TABLE I
SWITCHING SCHEME AND AVAILABLE VOLTAGE VECTORS IN EACH REGION

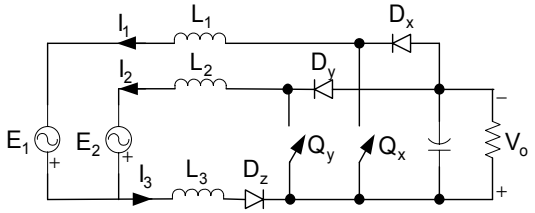
Region	Q1	Q2	Q3	Q4	Q5	Q6	Available voltage vectors
1	PWM	PWM	OFF	ON	PWM	PWM	V_5, V_6, V_1, V_8
2	ON	OFF	PWM	PWM	PWM	PWM	V_6, V_1, V_2, V_7
3	PWM	PWM	PWM	PWM	OFF	ON	V_1, V_2, V_3, V_8
4	PWM	PWM	ON	OFF	PWM	PWM	V_2, V_3, V_4, V_7
5	OFF	ON	PWM	PWM	PWM	PWM	V_3, V_4, V_5, V_8
6	PWM	PWM	PWM	PWM	ON	OFF	V_4, V_5, V_6, V_7

TABLE II
CIRCUIT PARAMETERS OF EQUIVALENT CIRCUIT IN FIG. 5.

Region	E_1	E_2	I_1	I_2	I_3	L_1	L_2	L_3	D_x	D_y	D_z	Q_x	Q_y
1	E_{ab}	E_{cb}	I_a	I_c	I_b	L_a	L_c	L_b	D1	D5	D4	Q2	Q6
2	E_{ba}	E_{ca}	I_b	I_c	I_a	L_b	L_c	L_a	D4	D6	D1	Q3	Q5
3	E_{bc}	E_{ac}	I_b	I_a	I_c	L_b	L_a	L_c	D3	D1	D6	Q4	Q2
4	E_{cb}	E_{ab}	I_c	I_a	I_b	L_c	L_a	L_b	D6	D2	D3	Q5	Q1
5	E_{ca}	E_{ba}	I_c	I_b	I_a	L_c	L_b	L_a	D5	D3	D2	Q6	Q4
6	E_{ac}	E_{bc}	I_a	I_b	I_c	L_a	L_b	L_c	D2	D4	D5	Q1	Q3



(a) circuits for regions 1/3/5



(b) circuits for regions 2/4/6

Fig. 5. Equivalent circuits of parallel-connected dual boost converter.

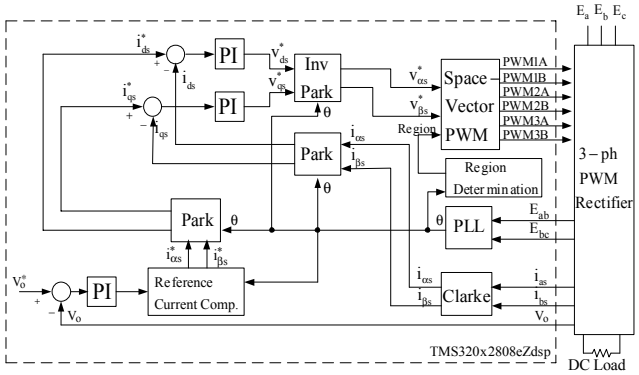


Fig. 6. Overall block diagram of 3-ph PWM rectifier with PFC.

C. Mathematical Model of Three-Phase PWM Rectifier and Required dq-axis Voltage References

According to Fig. 2, the abc voltage equations of three-phase PWM rectifier can be expressed as

$$E_a = L\frac{di_a}{dt} + V_{an} \tag{4}$$

$$E_b = L\frac{di_b}{dt} + V_{bn} \tag{5}$$

$$E_c = L\frac{di_c}{dt} + V_{cn} \tag{6}$$

where $L = L_a = L_b = L_c$.

The abc voltage equations (4)-(6) are then converted to the synchronously rotating dq-axis system using the phase voltage angle (θ), known as Park transformation.

$$\begin{bmatrix} f_{ds} \\ f_{qs} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-2\pi/3) & \cos(\theta+2\pi/3) \\ -\sin\theta & -\sin(\theta-2\pi/3) & -\sin(\theta+2\pi/3) \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{7}$$

Assuming that three-phase system be balanced, so the zero-axis variable is disappeared in (7). As a result, the dq-axis voltage equations of three-phase PWM rectifier are finally as

$$E_d = L\frac{di_{ds}}{dt} - \omega L i_{qs} + V_{ds} \tag{8}$$

$$E_q = L\frac{di_{qs}}{dt} + \omega L i_{ds} + V_{qs} \tag{9}$$

Next, the dc output voltage equation is simply derived as

$$i_o = i_C + i_R = C\frac{dV_o}{dt} + \frac{V_o}{R} \tag{10}$$

where the output current of rectifier (i_o) could be found in terms of three-phase line currents and switching functions of upper switches (Q_1, Q_3, and Q_5) as

$$i_o = Q_1 i_a + Q_3 i_b + Q_5 i_c \tag{11}$$

The αβ-axis current references are computed from the peak of reference currents (I_p^* , output of PI output voltage controller) and phase voltage angle (θ) from PLL as follows.

$$i_{\alpha s}^* = I_p^* \sin\theta \tag{12}$$

$$i_{\beta s}^* = -I_p^* \cos\theta \tag{13}$$

Then, these αβ-axis current references are transformed to the dq-axis current references as

$$i_{ds}^* = i_{\alpha s}^* \cos\theta + i_{\beta s}^* \sin\theta \tag{14}$$

$$i_{qs}^* = i_{\beta s}^* \cos\theta - i_{\alpha s}^* \sin\theta \tag{15}$$

When (12)-(15) are substituted into (14)-(15), the dq-axis current references become

$$i_{ds}^{*} = 0 \quad (16)$$

$$i_{qs}^{*} = -I_{p}^{*} \quad (17)$$

Consequently, the required dq-axis voltage references are found from (8)-(9) be substituted by (16)-(17), yields

$$V_{ds}^{*} = E_{d} + \omega L i_{qs}^{*} \quad (18)$$

$$V_{qs}^{*} = E_{q} - L\frac{di_{qs}^{*}}{dt} \quad (19)$$

Similar to the dq-axis current references (16)-(17), the dq-axis utility phase voltages are also $E_d = 0$ and $E_q = -\frac{E_p}{\sqrt{3}}$ because these three-phase current references and phase voltages are in phase to each other. Also, the i_{qs}^{*} is supposed to be constant, so its derivative is simply zero. Finally, the required dq-axis voltage references are found as

$$V_{ds}^{*} = -\omega L I_{p}^{*} \quad (20)$$

$$V_{qs}^{*} = -\frac{E_p}{\sqrt{3}} \quad (21)$$

It is obvious that both d- and q-axis voltage references are negative. Moreover, the d-axis voltage reference is varied according to dc load (I_p^{*}) whereas the q-axis voltage reference is theoretically constant. The outputs of the dq-axis current controllers should behave corresponding to (20)-(21).

III. Experimental results

The 3-ph PWM rectifier with PFC system depicted in Fig. 6 has been implemented on a 32-bit, fixed-point DSP based controller from Texas Instruments (TI), i.e., TMS320F2808eZdsp board. The system parameters are C = 2200μF, L_a= L_b = L_c = 10mH, and line frequency = 50 Hz. The PWM, ISR, and sampling frequencies are configured at 10 kHz. The testing data is conveniently stored in the on-chip memory of DSP. Then, it is exported as the text files from Code Composer Studio v3.1 (i.e., software development tool for TI DSP). These data files are then imported and easily plotted in Matlab. The experimental results are shown in Figs. 7 through 9. Firstly, three-phase PLL is investigated in terms of its response time. In Fig. 7, the computation of PLL is started nearly the peak of the measured line-line voltage, E_{ab}. The q-axis line-line voltage E_{qs} is controlled by PI controller and eventually approaches to zero when time is taken about 0.2 sec. (or 10 cycles). The lowest trace shows the PI output signal (U) which provides the additional positive frequency to accelerate or negative frequency to decelerate the computed PLL angle such that the PLL angle matches with the actual one. Since the fast PI gains are selected, so the waveform of U signal looks like on-off control.

Next, the start-up responses at 0.07 sec. are shown in Fig. 8. All six switches in rectifier are turned off before 0.07 sec. The phase voltage and line current (phase a) are apparently in phase to each other after the PFC mode is active. Notice that this phase voltage is constructed inside DSP by using PLL angle and computed amplitude of line-line voltage (E_p). The step-up/down responses of dc output voltage are also plotted in Fig. 9. The reference dc output voltage is stepped up from 100V to 150V at time = 0.1 sec, then stepped down back to 100V volt at time = 0.4 sec. The phase voltage of three-phase source is 50V(peak) during this test. As expected, the dc output voltage can also be successfully controlled while the line current is maintaining in phase with the corresponding phase voltage. The settling time during step-up is much faster than one during step-down, resulting in a large transient line current. This implies that three-phase source is momentarily supplying the large input power to quickly charge the dc-bus capacitor during this transient. The dc-bus capacitor (C) would be discharged to reduce its voltage thru the load resistor (R) and three-phase source. When the desired dc output voltage is therefore reduced, the response time would depend on the time constant of RC. i.e., higher value of load resistor, longer settling time.

IV. Conclusions

In this paper, a three-phase space-vector based PWM rectifier with power factor control has been proposed and implemented on a fixed-point DSP based controller. The required dq-axis voltage references are also derived. The proposed algorithm of dc output voltage and unity power factor controls is mainly validated by lab testing. According to the experimental results, three-phase PLL response time is only about 0.2 sec. The goal of controlling both dc output voltage and unity power factor is satisfactorily achieved.

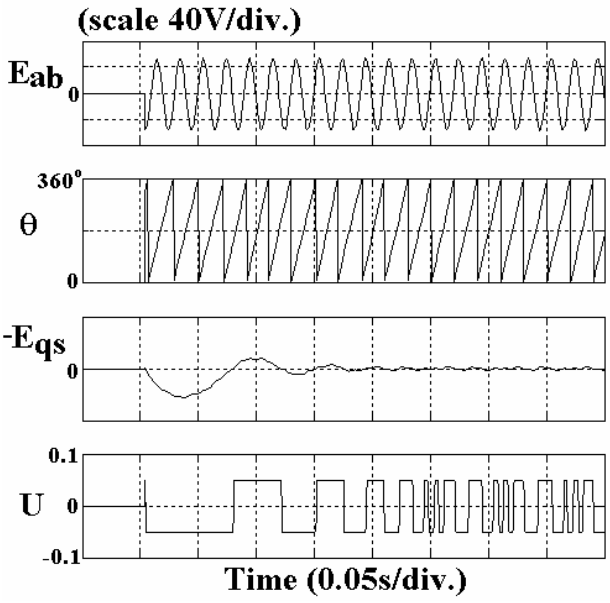


Fig. 7. Line-line voltage (E_{ab}), PLL angle, error signal ($-E_{qs}$), and PI output (U).

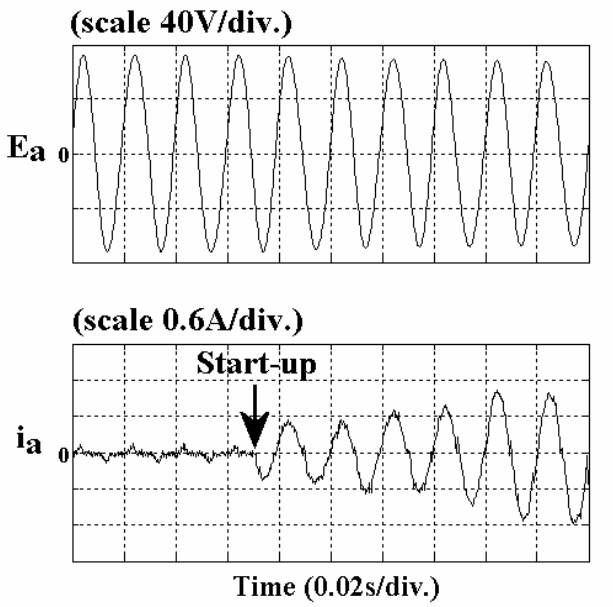


Fig. 8. Start-up phase-a voltage and line current (phase a).

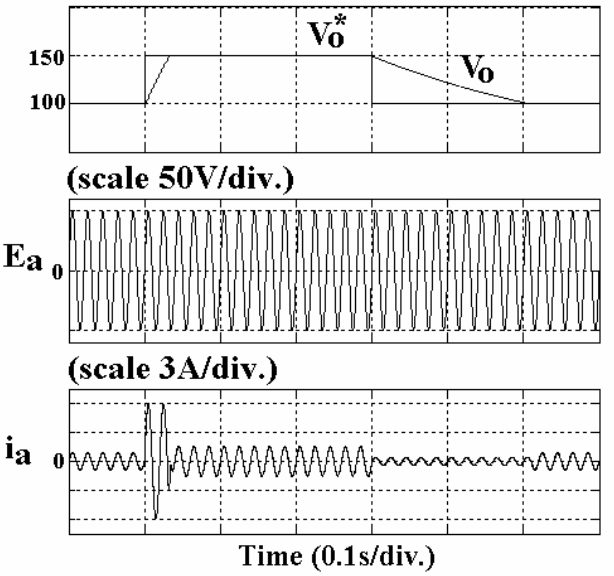


Fig. 9. DC output voltage step-up/down response, phase-a voltage, and line current (phase a).

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