

Power Flow Control with Static Synchronous Series Compensator (SSSC)

Nitus Voraphonpiput, Teratam Bunyagul, and Somchai Chatratana

Abstract— The Static Synchronous Series Compensator (SSSC) which is a Series FACTS Controller, becomes more attractive due to its superior abilities over the impedance-based series compensation. These superior abilities can only be achieved by appropriate control schemes and controller settings. This paper proposes two control schemes of the SSSC for the power flow control. The first scheme, which is called Reactance Emulation Scheme, the SSSC performs a function of the series impedance connected to the transmission line. This performance can be achieved by controlling the quadrature voltage of the SSSC in relation to the transmission line current and, the required series impedance compensation. The second control scheme, which is called Quadrature Voltage Control Scheme, the SSSC injects a quadrature voltage into the transmission line. Three modes of compensation can be achieved by controlling the phase relationship between the injected voltage and line current and the magnitude of the compensated voltage. Three modes of operations are capacitive compensation, inductive compensation, and reverse power flow. Conventional proportional plus integral (PI) controllers and sequential controls are used in the two control schemes. A 12- pulse voltage source converter was employed to represent SSSC operation. A 150 MVA SSSC was installed at a sending end bus of a simple two-bus 115 kV 50 Hz power system for the power flow control. Dynamic responses of the SSSC with two control schemes were investigated by the digital simulator. Simulation results illustrate effectiveness of the SSSC under both control schemes. Furthermore, the SSSC with quadrature voltage control scheme showed superior performance over the reactance emulation control scheme for its ability to reverse the power flow of the transmission line.

Keywords— SSSC, FACTS, Power Flow Control, Quadrature Voltage Control Scheme, Reactance Emulation Scheme

1. INTRODUCTION

The Static Synchronous Series Compensator (SSSC) or (S3C) is a series voltage source based Flexible AC Transmission System (FACTS) controller. The SSSC is usually combined with a Static Synchronous Compensator (STATCOM) and they are operated as a Unified Power Flow Controller (UPFC). However, STATCOM and SSSC can be designed to operate independently [1]. The SSSC can operate in the Direct Voltage Injection Mode when the STATCOM is not in service. The injected voltage phasor is always kept in quadrature with the transmission line current phasor. Thus, the SSSC provides purely reactive series compensation [2]. The active power flow of the transmission line can be regulated by controlling of the quadrature voltage of the SSSC.

This paper proposes two control schemes for regulating power flow of the transmission line. The first scheme which is known as Reactance Emulation Scheme (RES), the SSSC performs as additional series reactors or series capacitors of the transmission line. The power flow of the transmission line decreases when the SSSC emulates itself as series reactors. The power flow increases when the SSSC emulate itself as series capacitors.

The second scheme is known as Quadrature Voltage Control Scheme. In this scheme the SSSC performs as three-phase AC voltage source and produces voltage phasors, which are in quadrature with the line current phasors. The injected voltage can directly increase or decrease voltage drop across the

actual reactance of the transmission line. Consequently, the current flow and power flow of the transmission line can be increased or decreased.

2. PRINCIPLE OF OPERATION OF SSSC

The SSSC is generally connected in series with the transmission line with the arrangement as shown in Fig.1. The SSSC comprises a coupling transformer, a magnetic interface, voltage source converters (VSC) and a DC capacitor.

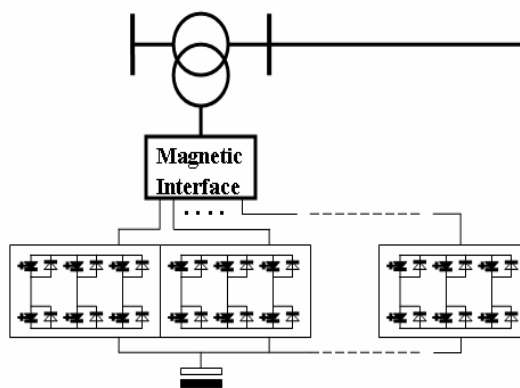


Fig.1. Diagram of general arrangement of SSSC with the transmission line

The coupling transformer is connected in series with the transmission line and it injects the quadrature voltage into the transmission line. The magnetic interface is used to provide multi-pulse voltage configuration to eliminate low order harmonics. The VSCs are either two-level converter or three-level converter. One side of the VSC is connected to the magnetic interface while the other side is connected to the DC bus. The VSC generates six-pulse voltage waveform and it is combined into multi-pulse (12 pulses) voltage waveform by Wye-Delta connection of the magnetic interface. More pulses (24 or 36 pulses) can be achieved if zigzag transformers are used as the magnetic interface. The DC capacitor is used to maintain DC voltage level on the DC bus. This DC capacitor is selected to meet harmonic and economic criteria of the SSSC and the power system.

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The operating principle of the SSSC can be explained using the simple two-bus system with its associated voltage and current phasor diagram in Fig 2.

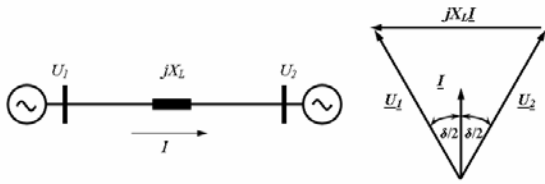


Fig. 2. Simple two-bus power system and phasor diagram

The active power flow between two buses can be expressed as

$$P_{12} = \frac{U_1 U_2}{X_L} \sin \delta \quad (1)$$

where P_{12} is the active power flow from Bus 1 to Bus 2
 U_1 is the magnitude of voltage at Bus 1
 U_2 is the magnitude of voltage at Bus 2
 δ is a phase angle difference between two buses
 X_L is the transmission line reactance

The magnitudes of bus voltages are normally regulated so that the variation lies within the acceptable range such as $\pm 5\%$. The phase angle difference between two buses (δ) is normally low to satisfy the angle stability condition. Therefore, the active power flow mainly depends on the line reactance (X_L).

If the SSSC is series-coupled to the transmission line, it will perform as controlled voltage source. A single line diagram and the phasor diagram of a transmission line with the series-compensated controllable voltage source are presented in Fig. 3.

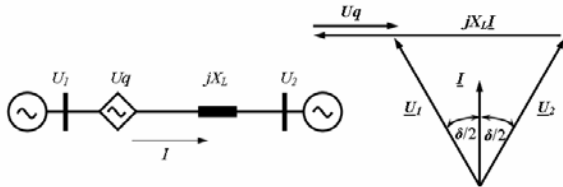


Fig.3 Two-bus system with the controllable voltage source

The active power flow between two buses (P_{12}) of the compensated transmission line is now expressed as

$$P_{12} = \frac{U_1 U_2}{X_L} \sin \delta + \frac{U_1 U_q}{X_L} \cos \left(\frac{\delta}{2} \right) \quad (2)$$

where U_q is the quadrature voltage injected into the transmission line.

It can be observed from (2) that with the same line parameters as in (1) (namely U_1 , U_2 , δ , and X_L), the active power flow (P_{12}) can be increased or decreased by assigning positive or a negative value to U_q . The relationship between active power and the power angle is shown in Fig. 4 for different values of U_q . Note that at a specific δ angle, for example $\delta = 30^\circ$, the active power flow (P_{12}) for $U_q = 0$ is 0.5 p.u. If $U_q = 0.5$ p.u. is added to the line at this angle, the power can be increased to 1.0 p.u. With $U_q = -1.0$ p.u. the power can even be reversed to -0.5 p.u. It should be noted here that the results, shown in Fig. 4, were made on the theoretical basis, to indicate the possibility of control range. Physical rating of components, saturation, and the

cost of investment will normally limit the range of the operation in practice.

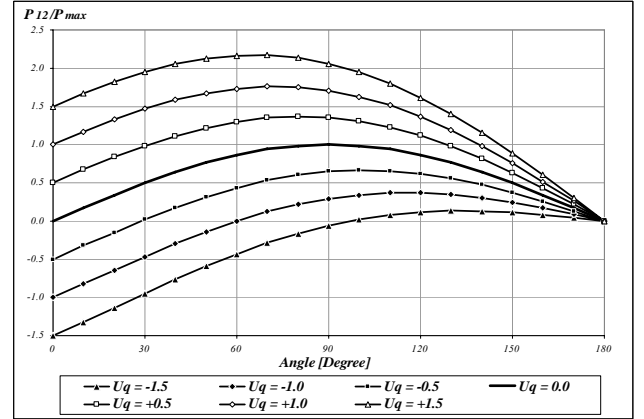


Fig.4. Power angle curve of the compensated transmission line with controllable series voltage source

The magnitude of the quadrature voltage (U_q) is directly proportional to the voltage of the DC capacitor in Fig. 1. The DC capacitor can be increased or decreased by a small shift of switching angle (firing angle) of the VSC.

3. REACTANCE EMULATION SCHEME

The SSSC can also perform a function of series impedance connected to the transmission line. This performance can be achieved by controlling the quadrature voltage of the SSSC in relation to the transmission line current and, the required series impedance compensation.

The controllable series impedance compensator, which is inserted into the transmission line, can be viewed as a means to decrease the reactive line impedance. A single line diagram and phasor of a transmission line with a series impedance compensation is shown in Fig. 5.

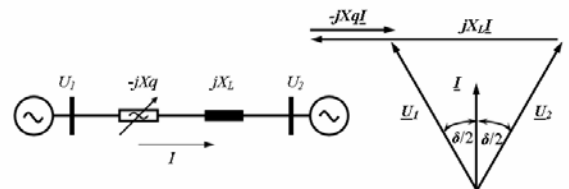


Fig. 5 Two-bus system with series impedance compensation

The total transmission line impedance becomes $X_L - X_q$ and the active power flow can be increased. The active power flow between two buses with series impedance compensation can be expressed as

$$P_{12} = \frac{U_1 U_2}{X_L (1 - k)} \sin \delta \quad (3)$$

where X_q is the required series impedance compensation.

k is the compensation ratio of X_q over X_L , $k = \frac{X_q}{X_L}$.

The power equation (3) can be plotted the power angle curve in Fig.6. The power angle curve shows that power flow of the transmission line is increased with the positive compensation ration (k) and it is decreased when the compensation ration (k) is negative values.

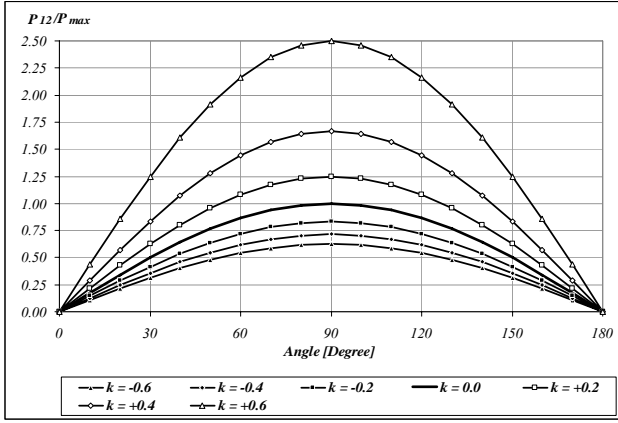


Fig. 6. Power angle curve of the compensated transmission line with the controllable series impedance

The power flow of the transmission line can be represented again as a function of the compensation ratio (k) in Fig. 7. It can be seen that the active power flow (P_{12}) decreases when k is negative. This behavior means that the controllable series impedance performs as a series inductor. On the contrary, the active power flow increases when k is positive. The controllable series impedance performs as a series capacitor. The active power flow can also be reversed when the compensation ratio k is more than one. In the transmission line point of view, the total reactive line impedance is now capacitive. Moreover, it can also be observed from Fig. 7 that the operating point of this system cannot be found when the compensation ratio k equals one because of the resonance between X_L and X_q . It results in discontinuous operating curve and the power flow reversal mode is difficult to operate.

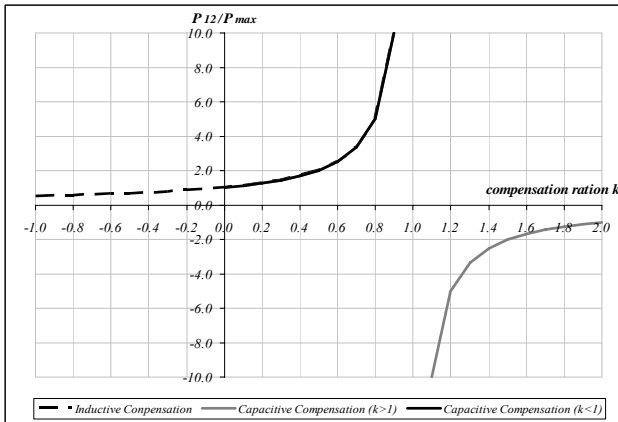


Fig. 7. Relation between power flow and compensation ratio k

From the transmission line standpoint, the controllable voltage source and controllable series impedance are employed to increase the voltage across the impedance of the given physical line and thereby increasing the line current and the transmitted power. It is important to note that the important parameter is the voltage across the physical line. It follows therefore that the power regulation can also be achieved if both series compensation are provided by a synchronous AC voltage source.

The Reactance Emulation Scheme (RES) is similar to the conventional series compensation. The SSSC performs itself as a series impedance of the transmission line. Therefore, the injected quadrature voltage (U_q) is a function of the transmission line current (I) and the required series impedance compensation (X_q). The quadrature voltage command (U_q^*) can be described as

$$U_q^* = IX_q^* \quad (4)$$

where U_q^* is the quadrature voltage command.

I is the transmission line current.

X_q^* is the required series impedance compensation.

The Reactance Emulation Scheme (RES), which is modified from [3], is represented in Fig. 8. The quadrature voltage command can be calculated from the required impedance compensation command (X_q^*) and transmission line current (I) as shown in (4). The PI-controller is selected to regulate DC voltage according to the DC voltage command (U_{dc}^*), which is calculated from the absolute value of the quadrature voltage command (U_q^*). Consequently, the three-phase line current is measured and fed into the current magnitude calculation block. Result of the magnitude calculation block is fed into the PLL to determine the phase angle of the current (θ_i).

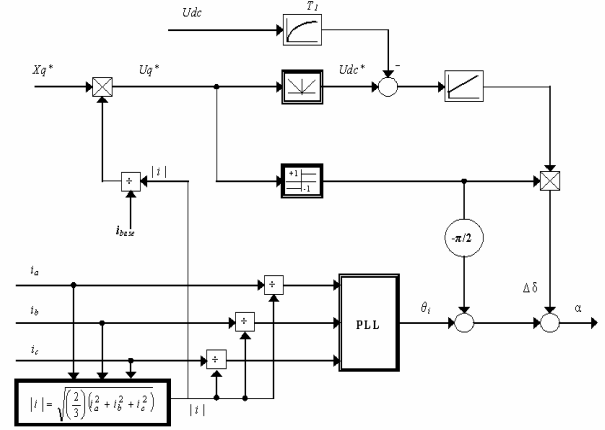


Fig. 8. Block Diagram of Reactance Emulation Scheme

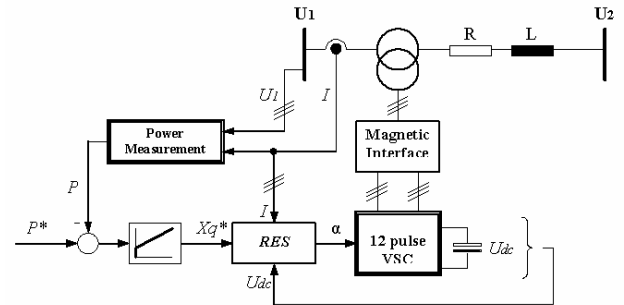


Fig. 9. Block Diagram of Power Flow Control with RES

The diagram of power flow control is shown in Fig. 9. It is the cascaded control with the inner loop representing the Reactance Emulation Scheme (RES). The outer loop consists of the power measurement block and a PI-controller. The power flow of the transmission line is measured and compared with the power command (P^*). The result of comparison is fed into the PI-controller, which generates the appropriate required impedance compensation command (X_q^*) for the RES block.

4. QUADRATURE VOLTAGE CONTROL SCHEME

When consider the equivalent circuit of a transmission line with SSSC in Fig. 10, the voltage sources U_1 and U_2 represent voltages of the sending end and the receiving end, respectively. The series compensated controllable AC source (U_q) is the equivalent circuit of SSSC. The transmission line is represented by a resistor (R) and an inductor (L). The transmission line current is defined to flow from Bus 1 to Bus 2. Phasor diagram of the transmission line with SSSC in three operation modes are shown in Fig. 11. It should be noted that all phasor diagrams in Fig. 11 were not drawn to scale. They were exaggerated to show the effect of compensation on the current flow. In normal operation, the voltage phasor \underline{U}_1 leads the voltage phasor \underline{U}_2 with

δ degrees. The voltage across the transmission line is represented by phasor \underline{U}_T , which consists of the voltage across the inductor \underline{U}_{XL} and the voltage across the resistor \underline{U}_R . The phasor \underline{I} represents transmission line current.

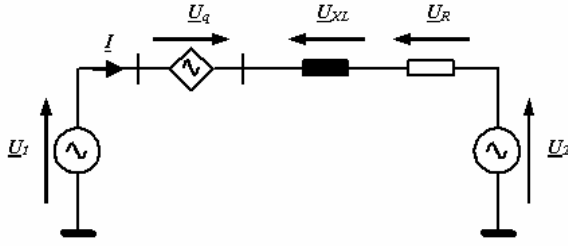


Fig.10. Equivalent circuit of SSSC system

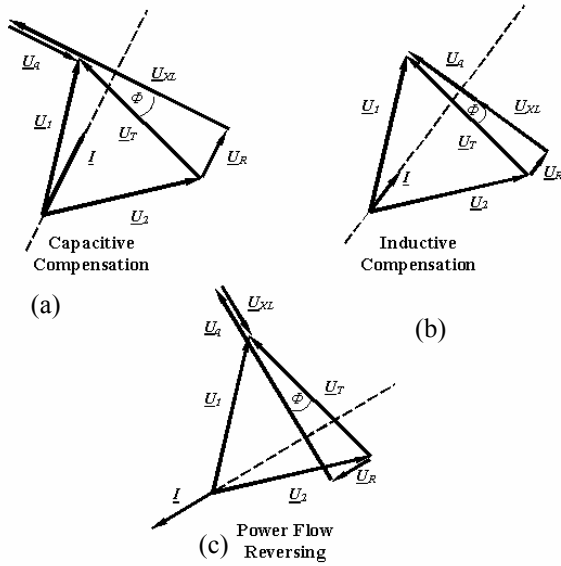


Fig. 11. Phasor Diagram of three operation modes (a) capacitive compensation (b) inductive compensation and (c) power flow reversing

The capacitive compensation by SSSC is shown in Fig.11 (a). The phasor quadrature voltage \underline{U}_q is located in the opposite direction of the phasor \underline{U}_{XL} and \underline{U}_q lags the current phasor \underline{I} by 90° . For the same total voltage drop \underline{U}_T , the voltage phasor across line reactance (\underline{U}_{XL}) increases and results in the increase of the transmission line current.

The inductive compensation is shown by the phasor diagram in Fig. 11 (b). The quadrature voltage is located in the same direction of the phasor \underline{U}_{XL} and \underline{U}_q leads the current phasor \underline{I} by 90° . For constant \underline{U}_T , the phasor \underline{U}_{XL} will decrease. The transmission line current reduces and results in the reduction of the power flow.

The ability of SSSC to reverse power flow is demonstrated by the phasor diagram in Fig. 11 (c). The operation is similar to the inductive compensation but the VSC voltage will be further increased until it is larger than magnitude of \underline{U}_{XL} . For constant \underline{U}_T , \underline{U}_{XL} reverses its direction and the current phasor \underline{I} must reverse and hence power flow reverses.

The Quadrature Voltage Control Scheme (QVCS) as shown in Fig. 12, offers three operation modes. The QVCS consists of a measurement system, controller, and logical switch block. The main function of the control loop is to maintain DC voltage according to the quadrature voltage command (U_{q^*}). The DC voltage (U_{dc}) is measured and compared with the DC voltage command (U_{dc}^*), which is calculated from an absolute value of the quadrature voltage command ($|U_{q^*}|$). The result of

comparison is fed into a proportional plus integral controller (PI-controller). The PI-controller is used to control the DC voltage by generating appropriate phase angle signal ($\Delta\delta$). Parameters of the PI-controller, which are the proportional gain (K_p) and the integrator time constant (T_n), are tuned to achieve fast dynamic response of the inner control loop. There are two logical switches which arrange the switching angle of the SSSC according to each operating mode. The logical switches are controlled by signal from the quadrature voltage command (U_{q^*}). The magnitude and polarity of the quadrature voltage command (U_{q^*}) is determined in the upper part of the diagram in Fig. 12.

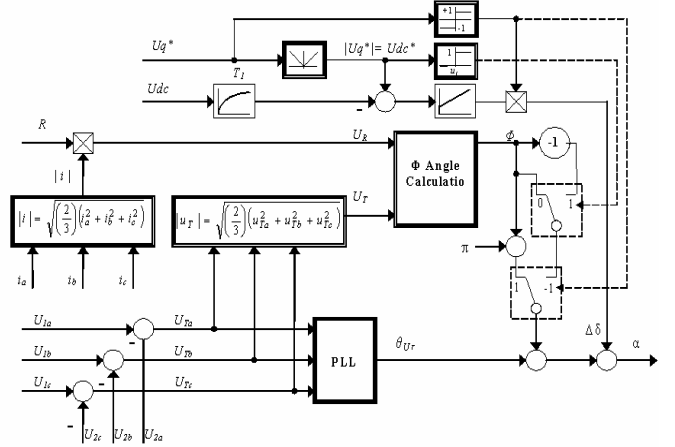


Fig.12 Block Diagram of Quadrature Voltage Control Scheme

The three-phase bus voltage of Bus 1 and Bus 2 are measured and used for the calculation of the voltage drop of the transmission line (U_T). The Phase Locked Loop (PLL) uses these signals to calculate phase angle (θ_{UT}). The magnitude $|U_T|$ is also calculated from the three-phase U_T signals (U_{Ta} , U_{Tb} , U_{Tc}). The three phase line currents are measured and used for the calculation of resistive voltage drop (U_R). The signals $|U_T|$ and U_R are used to calculate the angle Φ .

The conditions of command U_{q^*} and firing angle for three operation modes are given below:

1. Capacitive compensation: $U_{q^*} > 0$
 $\alpha = \Delta\delta + \theta_{UT} + \Phi + \pi$
2. Inductive compensation: $U_{q^*} < 0$ and $|U_{q^*}| < U_T$
 $\alpha = \Delta\delta + \theta_{UT} + \Phi$
3. Reversing power flow: $U_{q^*} < 0$ and $|U_{q^*}| > U_T$
 $\alpha = \Delta\delta + \theta_{UT} - \Phi$

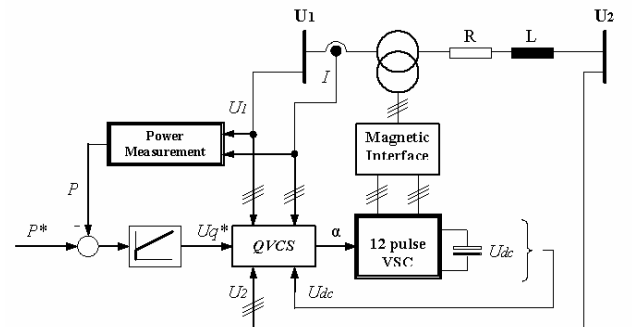


Fig. 13 Block Diagram of Power Flow Control with QVCS

The block diagram of the cascaded power flow control is shown in Fig.13. The quadrature voltage control scheme (QVCS), which is contained inside the block diagram in Fig.12,

forms an inner loop of Fig. 13. The power flow is calculated from voltage and current at Bus 1 by a power measurement block. Only one PI-controller is used in the outer loop to control the power flow of the transmission line. This controller generates the voltage command Uq^* .

5. SIMULATION RESULTS

The circuit diagram of two-bus 115 kV 50 Hz system with SSSC as shown in Fig. 14 was simulated with PSCAD/EMTDC. The transmission line parameters are $L = 36.4$ mH and $R = 0.3997 \Omega$. The system base MVA is 200 MVA and the rating of SSSC is 150 MVA. The rating of the coupling transformer is 150 MVA and 20kV/20kV voltage winding. The magnetic interface comprises two banking transformers which the primary windings are connected in series with the coupling transformer while the secondary windings are connected in Wye and Delta, respectively. The Wye and Delta connection are connected to two-level voltage source converter. The rating of both transformers, which act as the magnetic interface, are 25 MVA and voltage windings are 10 kV/5.77 kV and 10 kV/10 kV respectively. All transformers are represented with 5% impedance. A 1,500 μ F capacitor is selected for in this case. Phase voltage at sending end bus leads the receiving end bus by 10 degrees. The SSSC base voltage is 16.365 kV (peak). The system base phase voltage is 93.9 kV (peak). The transmission line base current is 1.429 kA. The base DC voltage is 9.09 kV.

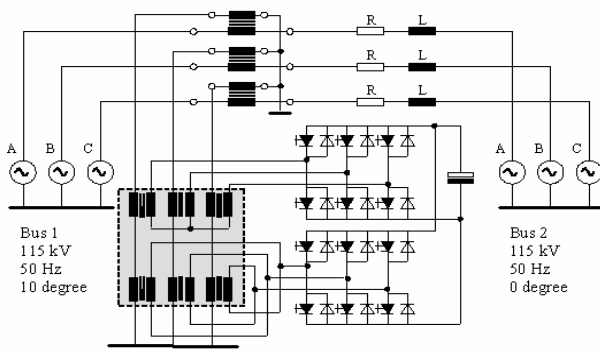


Fig. 14. The circuit diagram of two bus 115 kV 50 Hz system with SSSC

5.1 Reactance Emulation Scheme (RES)

The simulation results of the Reactance Emulation Scheme (RES), which presented in Fig.8 and Fig.9, were shown in Fig. 15 to Fig.22. The system and SSSC under the RES was tested with six events, which occur at 1.0 sec., 1.5 sec., 2.0 sec., 2.5 sec., 3.0 sec. and 3.5 sec. respectively. Power flow of the transmission line was first regulated at 1.5 p.u.. The power flow command (P^*) was changed from 1.5 p.u. to 1.25 p.u. at $t=1.0$ sec. Power flow of the transmission line decreased to 1.25 within 0.1 sec. and took 0.2 sec. to settle. The power flow command (P^*) was changed to 1.5 p.u. again at 1.5 sec. The third event was the same as the first one. The fourth event occurred at 2.5 sec. The power flow command (P^*) was changed from 1.25 p.u. to 0.75 p.u. at $t = 1.5$ sec. Power flow of the transmission line reduced to 0.75 p.u. within 0.1 sec. and took 0.2 sec. to settle. The fifth event occurred at $t = 3.0$ sec, when power flow of the transmission line was reduced from 0.75 p.u. to 0.5 p.u. It could be observed that there is no overshoot of the power flow at this event. Moreover, it could be seen from Fig.15 that the dynamic response in each event was not the same. This is because of the nonlinear function resulted from multiplication of required impedance compensation and transmission line current. The power reversing mode could not be performed in this scheme.

Active power (P_{SSC}) and reactive power (Q_{SSC}) of the SSSC during all operations with RES are shown in Fig. 16. The SSSC generated reactive power during the first event to the third

event. It absorbed reactive power at the fourth event to the sixth event. It could be seen that the active power consumed by SSSC was very small.

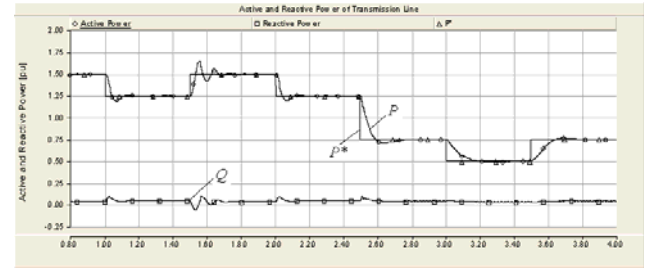


Fig. 15. Active power and reactive power flow of the transmission line (RES)

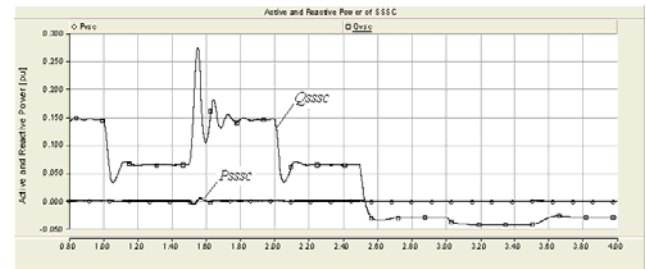


Fig. 16. Active power and reactive power flow of SSSC

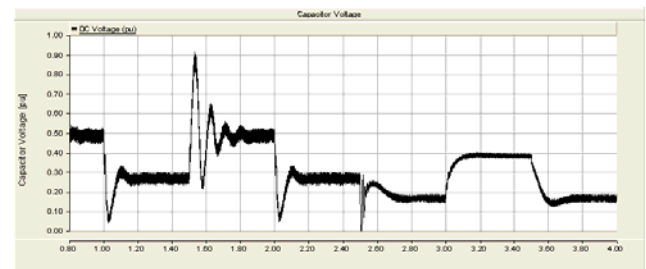


Fig. 17. DC capacitor voltage

The DC capacitor voltage is shown in Fig.17. It varied according to the power flow command (P^*). It can be observed that DC voltage ripple of increasing power flow operation (the first event to the third event) was higher than decreasing power flow operation (the fourth event to the sixth event).

The voltage waveform of the sending end bus (U_I), the transmission line current waveform (I) and the injected quadrature voltage waveform (Uq) of the first event up to the sixth event, except the third event, were presented in Fig. 18 to Fig. 22. It can be seen that the injected quadrature voltage (Uq) could increase and could decrease its magnitude within 1 cycle. Moreover, changing the phase angle from the lagging phase angle to the leading phase angle could be achieved within 1 cycle, as well. However, the response time of the transmission line current and the injected quadrature voltage took 8-10 cycles to settle.

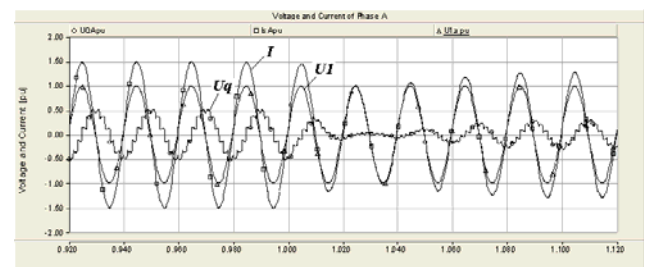


Fig.18 Voltage (U_I), current (I) and quadrature voltage (Uq) during the first event (phase A)

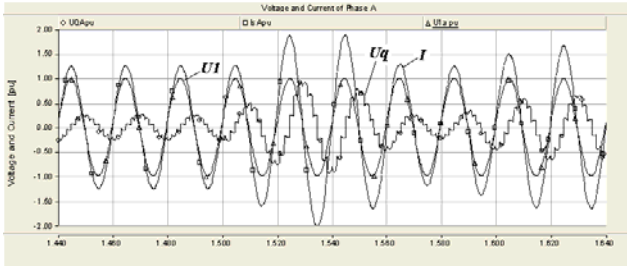


Fig.19 Voltage (U_l), current (I) and quadrature voltage (U_q) during the second event (phase A)

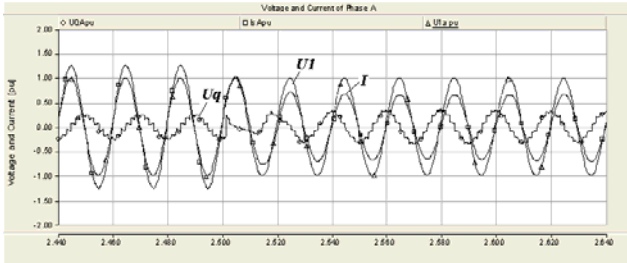


Fig.20 Voltage (U_l), current (I) and quadrature voltage (U_q) during the fourth event (phase A)

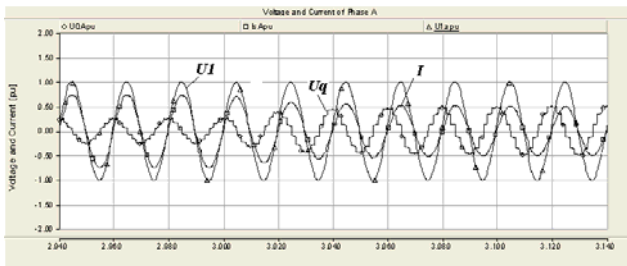


Fig.21 Voltage (U_l), current (I) and quadrature voltage (U_q) during the fifth event (phase A)

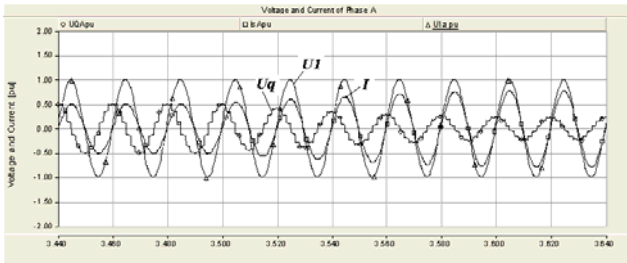


Fig.22 Voltage (U_l), current (I) and quadrature voltage (U_q) during the sixth event (phase A)

5.2 Quadrature Voltage Control Scheme (QVCS)

Diagram in Fig. 12 and Fig. 13 was created on PSCAD/EMTDC and applied to the system in Fig.15 for QVCS. The QVCS was tested with five events and simulation results were shown in Fig. 24 to Fig.31. The SSSC controlled power flow of the transmission line at 1.25 p.u. The first event occurred at 1.5 sec. The power flow command (P^*) was changed from 1.25 p.u. to 1.5 p.u. The power flow of the line increased to the set point value within 0.1 sec and settled at $t = 1.8$ sec. The second event occurred at 2.0 sec., when the power flow command (P^*) was reduced to 1.25 p.u. The SSSC performed as a capacitive compensation during the first and the second events.

The third event occurred at 2.5 sec., when the power flow command (P^*) was reduced further to 0.5 p.u. then the SSSC performed as inductive compensation. The power flow took 0.2 sec. to settle to the new value of 0.5 p.u.

The fourth event and the fifth event were power reversing mode. It could be seen that the power flow of the line reduced to -0.5 p.u. at $t = 3.0$ sec. and then returned to 0.5 p.u. at $t = 3.5$ sec. It could also be observed that the reactive power flow of the transmission line changed very little during the whole operation.

The dynamic responses of the power flow of the transmission line are shown in Fig. 23.

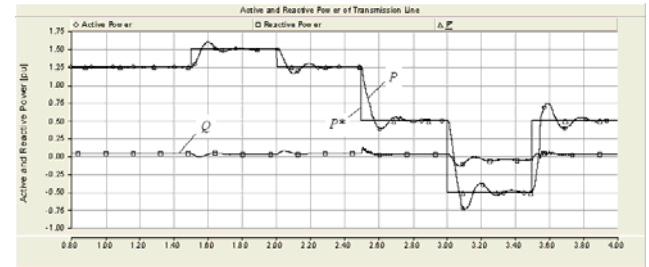


Fig. 23. Active power and reactive power flow of the transmission line (QVCS)

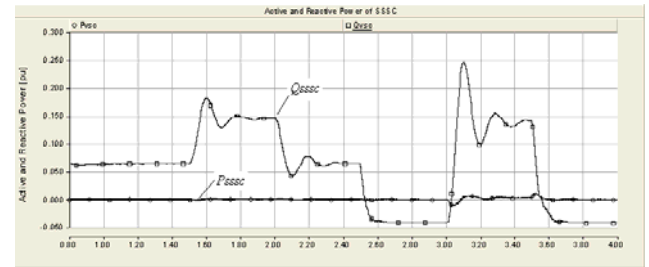


Fig. 24. Active power and reactive power flow of SSSC

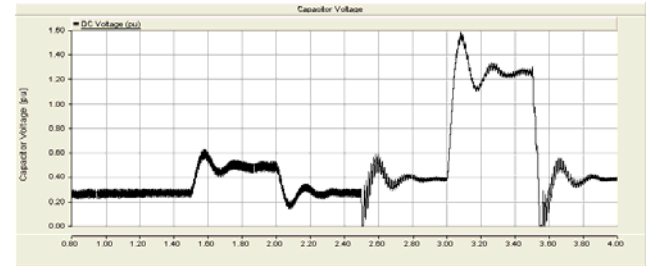


Fig. 25. DC capacitor voltage

The active power (P_{SSSC}) and the reactive power (Q_{SSSC}) response of the SSSC during all events are shown in Fig. 24. The SSSC generated reactive power (capacitive compensation) during the first event and the second event. It absorbed reactive power (inductive compensation) during the third event and generated the reactive power again when it performed in power reversing mode. It could also be seen that the active power of the SSSC was very small because the SSSC consumed active power only to maintain internal losses of the converters and the transformers.

The DC capacitor voltage responses are shown in Fig. 25. It varied due to the quadrature voltage command (U_q^*). It could be observed that the DC capacitor voltage was higher than 1.0 p.u. during 3.0 sec. to 3.5 sec. because the SSSC performed in the power reversing mode at that time.

The voltage waveform of the sending end bus (U_l), the transmission line current waveform (I) and the injected quadrature voltage waveform (U_q) during five events were presented in Fig. 26 to Fig. 30.

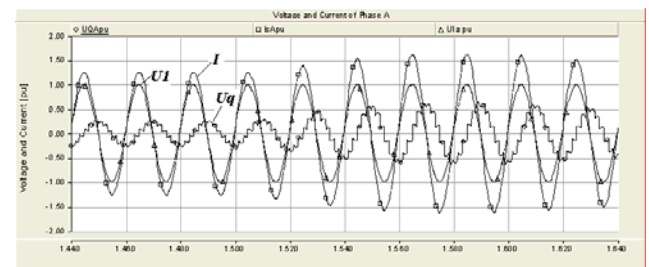


Fig.26 Voltage (U_l), current (I) and quadrature voltage (U_q) during the first event (phase A)

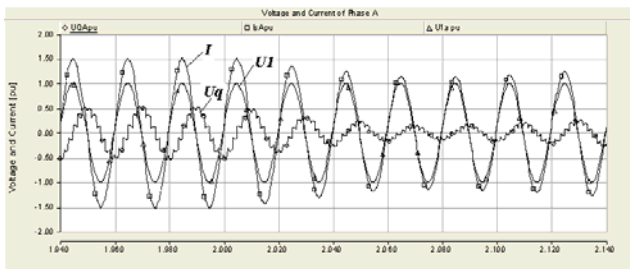


Fig.27 Voltage (U_1), current (I) and quadrature voltage (U_q) during the second event (phase A)

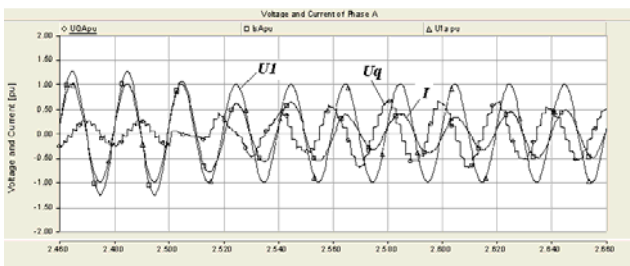


Fig.28 Voltage (U_1), current (I) and quadrature voltage (U_q) during the third event (phase A)

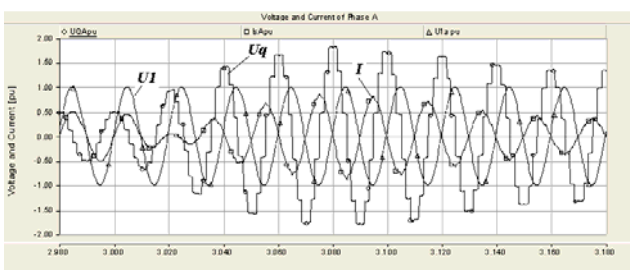


Fig.29 Voltage (U_1), current (I) and quadrature voltage (U_q) during the fourth event (phase A)

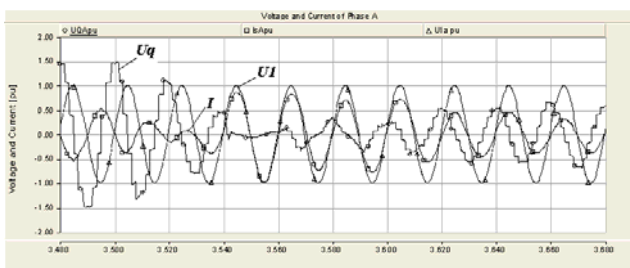


Fig.30 Voltage (U_1), current (I) and quadrature voltage (U_q) during the fifth event (phase A)

The transmission line current (I) could respond within one cycle and it took approximately 8-10 cycles to settle. Phase of the transmission line current (I), which was shown in Fig.29 and Fig.30, were reversed because the injected quadrature voltage (U_q) was higher than the voltage drop of the physical line. The injected quadrature voltage (U_q) was not a perfectly sinusoidal waveform because the 12-pulse voltage source converter was applied in this case.

The injected quadrature voltage lagged the transmission line current in Fig. 26 and Fig. 27. It changed to lead the transmission line current in Fig. 28. It lagged the transmission line current again when it performed power flow reversing mode, which was shown in Fig. 29. However, it could be observed in Fig.30 that the injected quadrature voltage led sending end voltage even the SSSC was inductive compensation or power reversing mode.

6. CONCLUSION

The principle of operation and the Quadrature Voltage Control scheme of a Static Synchronous Series Compensator (SSSC) for the power flow regulation was presented. This paper also presented two control schemes for SSSC which are the

Quadrature Voltage Control Scheme (QVCS) and the Reactive Emulation Scheme (RES), for the power flow regulation. Theoretical analysis and simulation results with PSCAD/EMTDC showed that the SSSC can effectively regulate the active power flow of the transmission line. Active power could be increased and decreased effectively with the SSSC under the QVCS and the RES. Moreover, the SSSC with the QVCS showed the superior performance over the reactance emulation control scheme for its ability to reverse the flow of the transmission line power.

The dynamic responses of the voltage and current waveform were fast. It took 1 cycle in average to change the magnitude or to reverse the phase angle. It also took approximately 8-10 cycles to settle. It can be concluded that the SSSC with the two control schemes offers good performance for the power flow regulation.

However, this paper presented theoretical and possible control method of a SSSC. It should be noted that, many practical considerations in terms of component rating, saturation, range of operation, and harmonic contents have to be taken into account in the design and construction of the SSSC.

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