TWO STAGE 10-BIT ADC WITH DELAY-LINE TDC BASED SECOND STAGE

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Abstract

Two stage 10-bit Time based ADC is designed and verified in a commercial VLSI CAD tool. Simple VCO driven counter is used in the first stage as coarse, whereas TDC based second stage used for fine conversion. Each stage will give 5bit resolution and work concurrently during the conversion process. Delay-line/Flash TDC is used in the second stage because of its better conversion speed. Flash TDC output will be thermometer code. Hence, a thermometer to binary conversion stage is required. To make it simple and area efficient, ROM based Thermometer to Binary (T2B) converters are used in the final readout module. Average power dissipation of 1.155 mW for the overall system is measured and makes it suitable for low power applications.

Keywords: ADC, current starved VCO, delay line TDC, time to digital converter, time based ADC, time mode ADC

Introduction

In many electronic subsystems, Analog to Digital Converter (ADC) is a significant block. Due to continuous scaling in VLSI, ADC reference voltage and analog input range are now well within 1 Volt. Recent trends show that time-based ADCs are alternative data converters in low supply-voltage VLSI circuits. Non-stop scaling in VLSI is the main reason to go for mostly-digital low power data converters. Therefore, chip designers tend to move towards Time-based ADCs. Traditional Analog to Digital Converters convert analog input into its equivalent digital value. However, working principle of time-based ADC, involving in quantizing analog input into a time pulse and then digitized into digital code by using Time to Digital Converter (TDC).

In many cases having a single stage conversion will not yield better resolution. For some ADC architectures, it is a trade-off between area and resolution. Two stage ADCs are in trend from last decade. The first stage will be coarse, where conversion is roughly but quickly done. The second stage will do fine conversion and add additional bits by converting the first stage residue. Few architectures (Gupta *et al*., 2011;) followed a general architecture as shown in Figure 1. The residue is generated and amplified for second stage conversion. Most of the blocks are analog and power hungry. Also, conversion of two stages takes place sequentially. In other words, the second stage has to wait for completion of first stage conversion and residue generation. Residue generation is again

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involved in digital to analog conversion followed by amplification.

Many modern VLSI systems try to avoid classical mixed-signal approach because of their bad scaling behaviour. i.e. Whether it is area scaling or voltage scaling, a whole redesigning of the system is required. On the other hand, TDC will measure *time* rather than voltage. So, irrespective of technology scaling, non-linearities will be under designer's control. Most of early architectures of TDCs are prototyped on FPGA because they are completely digital architectures. Fully digital circuits are most suitable for scaling. Hence, TDC is considered as a future data converter because of above mentioned reasons (Henzler, 2010).

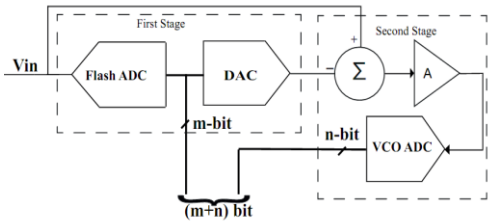


Figure 1. General structure of two stage ADC Proposed in Ghosh and Pamarti (2015); Gupta *et al*., (2011)

Time measurement can be broadly classified as direct method and indirect method. Figure 2 shows detailed classification of TDC architectures. Direct method includes many modern techniques; viz. Delay-line, Vernier delay-line, Vernier ring oscillator, Multipath gated ring oscillator, pulse shrinking technique etc. These architectures use reference clock or delay elements as the reference for conversion process. Indirect measurement (Rezvanyvardom *et al*., 2014) includes time-to-voltage-to-digital conversion. In other words, converting time to voltage and followed by Analog to Digital Conversion to get its digital equivalent. This mixed-signal TDC is called analog TDC or voltage-domain TDC. Indirect TDCs are not a subject of interest for those who are implementing mostly digital ADCs.

Time-based ADCs can be classified according to their working principle. The major time-based architectures are Slope and Integrating ADC, PWM ADC, Asynchronous ADC, Voltage Controlled Delay cell-based ADC and Voltage to Frequency conversion-based ADCs. A broad study of these architectures can be found in (Naraghi, 2009). Most of these are analog or mixed signal domain ADCs. Counter (TDC) was used for time to digital conversion. However, in recent time-based ADC architectures, advanced TDC topologies are used to make mostly digital ADC.

Time-based ADC proposed by Toraskar *et al*. (2016) employs pulse shrinking TDC. Pulse shrinking TDC topology is a simple and area efficient, but has a very slow conversion rate. There are several time-based ADCs implemented on FPGA. Time domain ADCs proposed in (Wu *et al.*, 2007; Mattada and Guhilot, 2019) utilize multiphase clock TDC. These Multiphase clock TDCs utilize PLL resources available within the FPGA. The ADC implemented by Hu *et al*. (2016) employs 2D Vernier TDC for high resolution. The ADC implemented in (Oh *et al.*, 2014) utilizes both time domain and voltage domain (also called as hybrid domain) employs pipelined TDC. Another two stage ADC presented by (Sharma *et al*. 2016) employs counter and delay line TDC.

Proposed Work

Figure 3 depicts proposed two stage TDC, where the *nutt interpolation* method is incorporated. Entire circuitry is designed using TSMC 0.3 µm technology and verified using *Spectre* simulator. Here, the first stage will be course and second stage is the fine conversion. Equation 1 mathematically expresses the *nutt* interpolation, where *n*Tclk*

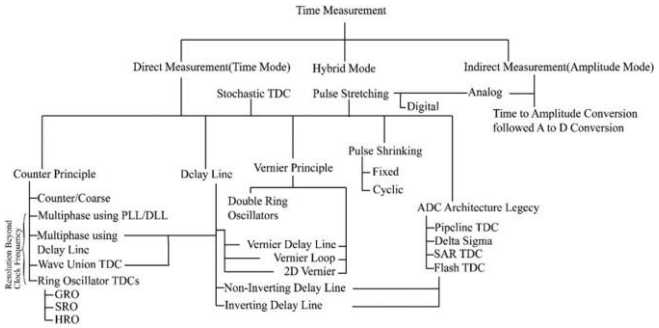


Figure 2. Classification of Time to Digital Converters

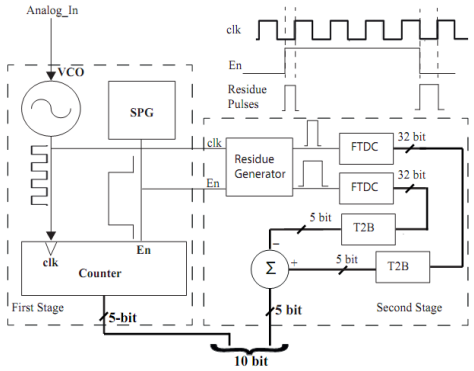


Figure 3. Proposed 2 stage ADC shows VCO based first stage and TDC based second stage

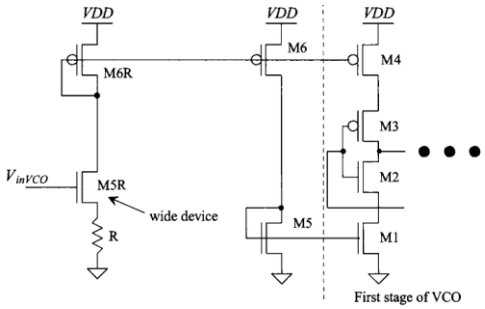
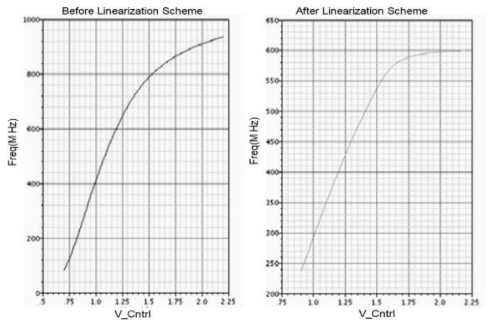
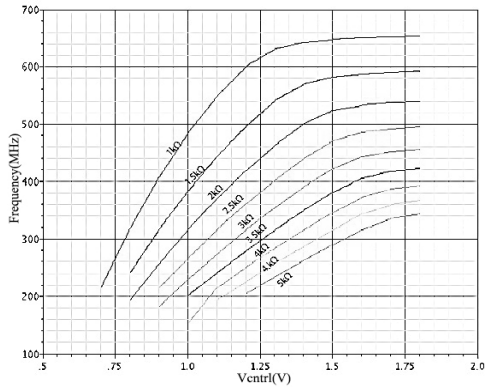


Figure 4. Current starved VCO mentioned in [3] with a linearization scheme



(a)



(b)

Figure 5. a) Linearity of VCO with and without linearity Scheme. b) Linearity of VCO frequency (MHz) with different values of R

represents coarse conversion using a counter. The change in analog input must be converted to change the time period of VCO. A counter driven by VCO will be enabled for a fixed amount of time. This stage will greatly enhance the measurement range. Instead of VCO, one can go for a fixed crystal oscillator. This will not enable user to change the frequency dynamically. Rather, a control-input option given to change VCO frequency, thereby adjustment of measurement range.

$$Tm = n * Tclk \pm T(Residues) \quad (1)$$

First stage or coarse stage consists of a counter, driven by VCO output and Single Pulse Generator (SPG). Here, SPG will generate fixed pulse width which enables the counter. Whereas VCO will trigger the counter with different clock frequencies proportional to the analog input voltage.

Second stage conversion for *residue* measurement will enhance the resolution. When it comes to present work, delay line TDC has been adopted. Delay-line TDC is also called as Flash TDC (FTDC). FTDC is well known for its simplicity and conversion speed. One drawback of delay-line TDC discussed in (Rezvanyvardom *et al*., 2014) is its exponentially increasing area-requirement as the number of bits increases. By incorporating coarse-fine stages one can overcome area overhead. i.e. Coarse stage is to enhance the range and fine stage to improve resolution. The proposed architecture is mostly digital and less power hungry and also suitable for scaling. An additional dynamic arrangement for its range without changing the measurement setup is an added advantage.

Design and Implementation

The proposed work can be divided into four major blocks. Following subsections cover each block along with necessary discussion.

Voltage Controlled Oscillator

Three stage current starved inverter chain is used as the VCO for the implementation. Figure 4 shows Current starved VCO with linearization

scheme mentioned in (Baker, 2009) is adapted in this work. Figure 5(a) shows the improvement in the linearity with the additional setup. To choose appropriate value for resistor *R*, a parametric simulation is carried out and presented in Figure 5(b). This allowed us to choose *R* between 4 kΩ to 5 kΩ for better linearity. Also, from the eye diagram, we found that, maximum period jitter is 2.7 ps.

There are some applications require ADC to be non-linear. For example, hearing aids. These wide range ADCs are also called as Logarithmic ADCs. Non-linear characteristics of the VCO makes the ADC output non-linear (Mattada and Guhilot, 2019).

Single Pulse Generator

Single Pulse Generator (SPG) is a monostable circuit, used in our earlier work (Toraskar *et al*., 2016). However, to reduce silicon area, delay elements are made to current starve. This in turn allows us to control SPG pulse width. To attain maximum pulse width *threshold voltage* (Vth) is applied for current starved delay line.

Residue Generator

To generate residue of the first stage a circuit from the previous work (Mattada *et al*., 2011) has been adopted. Schematic and simulation results for the same is as presented in Figure 6. The outputs of residue generator are then given to second stage for fine conversion. One can opt for time amplification (TA) (Shih *et al*., 2015) to stretch the residue before applying to the second stage. TA scheme improves further resolution at the cost of silicon area. However, present work doesn't incorporate TA scheme to limit ADC resolution to 10-bit. Equation 1 can be rewritten with respect to Figure 5 and expressed in Equation 2. The final calculation of Equation 2 can be done at the front-end.

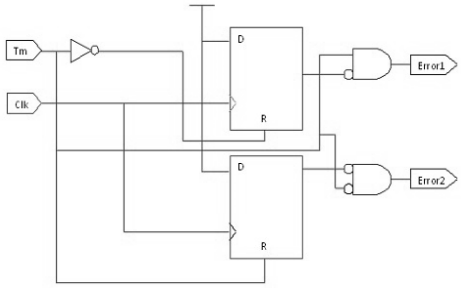
$$Tm = n * Tclk + Error1 - Error2 \qquad (2)$$

Flash TDC

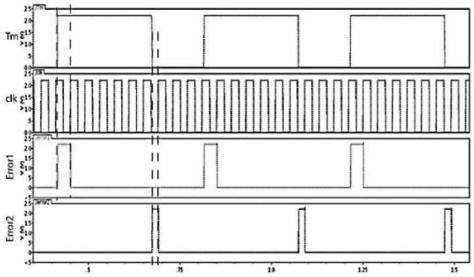
Figure 7(a) shows the general architecture of Flash TDC which is also known as Delay Line TDC. Two FTDCs are used to convert two tiny time residues in second stage. To decide the number of stages, it is necessary to identify maximum residue.

Delay of delay-element (normally buffer) in the delay-line decides the resolution of the TDC. The resolution of the present TDC is 213 ps and it is suitable for the proposed measurement setup. The delay element, i.e. Buffer in this work uses minimum size inverters. From the calculation we came to know that, 32 delay stages should suffice for worst case. There are different techniques to improve the resolution depends on the application requirement viz. increasing the size of transistors in the delay element or using an inverter instead of a buffer. However, it's a trade-off between resolution and area. Measured DNL and INL plots presented in Figure 7(b) and both lie within 1 LSB.

The FTDC output will be in thermometer code. Hence, thermometer-to-binary code conversion is essential. The simplest circuit for this conversion is ROM based Thermometer-to-Binary (T2B) encoder. Two Delay Line TDCs are deployed for 2 residue pulses. The fine stage results are then combined to form 10-bit output.



(a)



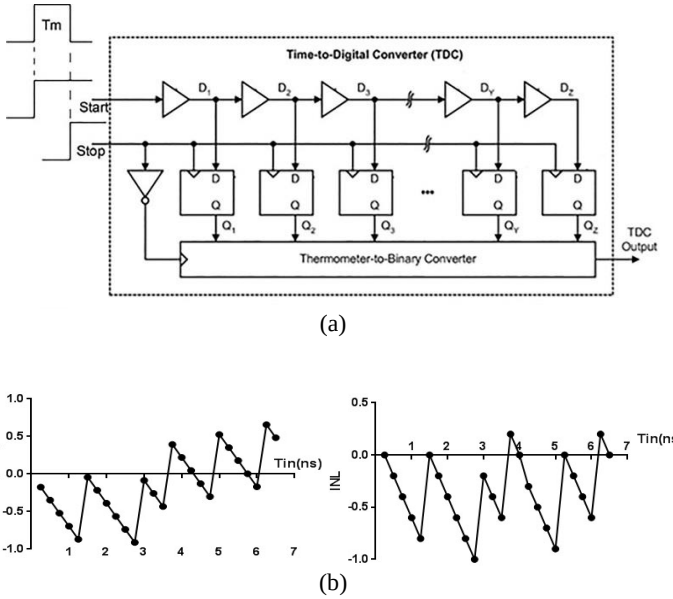
(b)

Figure 6. a) Schematic and b) Simulation results of residue generator

Results and Discussion

ADC characteristics are measured and presented in Figure 8. The final results after adding fine results is presented. One can observe the offset in the output code which propagated from coarse stage. Though the counter is 8-bit, the useful information after omitting offset will be within 5-bits. DNL of the overall system is within 1 LSB but INL went up to 1.3 LSB.

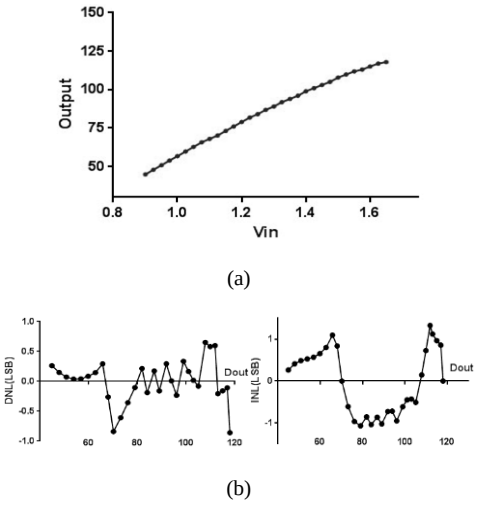
Power consumption chart for different blocks has been depicted in Figure 9. For each analog to digital conversion, an average power consumption of 1.155 mW has been recorded. The power consumption chart includes both static and dynamic



(a)

(b)

Figure 7. a) General architecture of Flash Time to Digital Converter (FTDC) b) Measured DNL and INL plots for 5bit FTDC



(a)

(b)

Figure 8. ADC Characteristics (a) Vin vs Dout-Coarse (b) DNL Plot (c) INL Plot

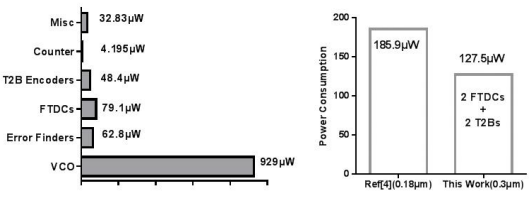


Figure 9. Power consumption chart of 2-stage ADC and Indirect vs FTDC power comparison

power. However, the major part of power is consumed by VCO i.e. 929 µW, which is part of the coarse stage. Originally VCO included to replace the crystal oscillator and make the IC to generate its own clock. So, 5-bit FTDC power consumption is compared with 5-bit TDC from the reference. This comparison chart is also shown in Figure9, where two 5-bit FTDCs consumes less power compared to one 5-bit TDC which uses the *indirect* technique. Hence, Indirect measurement and mostly-analog ICs probably consume more power compared to direct and mostly-digital time measurement architectures. Power consumption of the present work can be further improved by implementing the architecture with state-of-the-art VLSI technology.

Conclusions

Time based architectures are promising techniques for most of the future data converters problems. The current architecture has proven, simple yet effective way of implementing mostly-digital time-based ADCs. The proposed work has been designed and verified using a Cadence Tool with TSMC 0.3 µm technology. The resolution can be further enhanced by time-amplification or time stretching method at the SPG stage. The measured DNL was within ±1LSB and maximum INL was 1.3 LSB. The power consumption chart shows that, the present architecture is suitable for low power VLSI applications.

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