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A low-power low-error single-ended virtually-grounded-drain class AB switched-current memory cell

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Abstract

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A low-power low-error single-ended virtually-grounded-drain class AB switched-current memory cell is presented. The proposed circuit is relatively simple, based on a basic class AB SI memory cell and a level-shifted grounded-gate amplifier. No large differential circuitry and complicated clocking schemes are required. All charge-injection, clock-feedthrough and conduction errors are reduced. As a design example using 0.5-µm CMOS technology, the power consumption is 120 µW at the bias current of 25 µA and supply voltage of 2V. The optimal sampling frequency is at 45MHz. The SNR, SDR and SFDR are 59.7 dB, 61 dB and 73 dB, respectively. The total harmonic distortion is less than 0.4%. The transmission gain error and the DC offset current error are less than 0.025 and 0.75 µA, respectively. Demonstrations of a forward difference integrator and comparisons to other approaches are also presented.

Key words : switched-current technique, Class AB technique, memory cell, grounded-gate amplifier, offset compensation, charge injection, conduction error, low power, low error.

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วงจรหน่วยเก็บความจำสวิตซ์กระแสคลาสเอบีแบบโครงสร้างเชิงเดี่ยวและกราวน์เสมือน ใช้กำลังไฟน้อยและมีค่าความผิดพลาดต่ำ

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บทความนี้นำเสนอวงจรหน่วยเก็บความจำสวิตซ์กระแสคลาสเอบี ใช้กำลังไฟต่ำและมีความผิดพลาดน้อย แบบโครงสร้างเชิงเดี่ยวและกราวน์เสมือน วงจรที่นำเสนอใช้เทคนิคอย่างง่ายซึ่งประกอบด้วยวงจรหน่วยเก็บความจำสวิตซ์กระแสพื้นฐานคลาสเอบีและวงจรขยายสัญญาณ ดังนั้นจึงไม่ต้องการโครงสร้างเชิงคู่ที่มีขนาดใหญ่และสัญญาณควบคุมที่ซับซ้อนเช่นเดียวกับเทคนิคอื่น คุณสมบัติเด่นของวงจรคือสามารถลดค่ากระแสผิดพลาดในกระบวนการชักตัวอย่างเนื่องมาจากปัญหาการฉีดประจุ ปัญหาสัญญาณควบคุมหลุดลอดและปัญหาการนำสัญญาณกระแส ได้อย่างครบถ้วน ผลการจำลองการทำงานโดยใช้เทคโนโลยีซีมอสขนาด 0.5 ไมโครเมตร ที่กระแสไบแอส 25 ไมโครแอมแปร์และความต่างศักย์ไฟฟ้าขนาด 2 โวลต์ สามารถใช้กำลังไฟฟ้าต่ำเพียง 120 ไมโครวัตต์ นอกจากนี้ความถี่ของการชักตัวอย่างที่เหมาะสมมีค่า 45 เมกะเฮิรตซ์ ค่าสัญญาณต่อสัญญาณรบกวนและค่าสัญญาณต่อความเพี้ยนมีค่า 59.7 และ 61 เดซิเบล ตามลำดับ ค่าความเพี้ยนรวมมีค่าน้อยกว่า 0.4% ค่าความผิดพลาดจากการนำสัญญาณและกระแสอ๊อปเซ็ต มีค่าน้อยกว่า 0.025 และ 0.75 ไมโครแอมแปร์ตามลำดับ ในบทความนี้ยังได้แสดงวงจรอินทิเกรเตอร์ที่พัฒนาจากวงจรหน่วยเก็บความจำสวิตซ์กระแสที่นำเสนอและแสดงการเปรียบเทียบคุณสมบัติของวงจรหน่วยเก็บความจำสวิตซ์กระแสที่นำเสนอกับบทความอื่นที่เคยนำเสนอมาแล้วอีกด้วย

ภาควิชาการสื่อสาร อุปกรณ์วัดและระบบควบคุม สถาบันเทคโนโลยีนานาชาติสิรินธร มหาวิทยาลัยธรรมศาสตร์ ศูนย์บางกะดี 131 หมู่ 5 ถนนติวานนท์ ตำบลบางกะดี อำเภอเมือง จังหวัดปทุมธานี 12000

A switched-current (SI) memory cell typically provides a half-period delay of a current for a variety of applications such as in discrete-time filters or in sigma-delta analog-to-digital converters (Toumazou *et al*.,1993). Generally, two basic categories are the 1st-generation and the 2nd-generation SI memory cells. Although the 1st-generation SI memory cell offers a low level of transient glitches (Sinn and Roberts, 1994) and a readily adjustable current gain (Yang and Masry, 1994), the need for two transistors is vulnerable to mismatch errors and more power consumption. Alternatively, the 2nd-generation SI memory cell employs a single memory transistor in order to avoid the mismatch errors and reduce power consumption (Battersby and Toumazou, 1991).

However, associated problems in the 2nd- generation SI cell are not only the presence of large amplitude transient glitches but also the direct output where a unity current gain is not readily adjustable. Although the transient glitches can be reduced through a three-phase clock scheme (Oliaei and Loumeau, 1995), the additional sophisticated clock is required. The adjustable current gain can alternatively be possible through an additional mirrored transistor, but this leads to the undesirable mismatch errors and more power consumption as previously encountered in the 1st-generation SI memory cell. As lower power consumptions and smaller chip area are preferable towards the future CMOS technologies, the 2nd-geneation SI memory cell has consequently been of much interest compared with those 1st- generation SI memory cells (Goldenberg *et al*., 1994).

Both generations traditionally employ class A techniques and therefore limit the signal handling capability to no more than a bias current(Oliaei and Loumeau,1998). Larger signal swings require larger bias currents leading to more power sconsumption. Recently, class AB techniques for SI memory cells based on either the 1st-generation (San-Um *et al*., 2004) or the 2nd-generation (Srowik and Schuffny,

1999) have been developed for lower power consumption as a signal swing in the class AB techniques can be in excess of the bias current (Oliaei and Loumeau, 1998; Srowik and Schuffny, 1999). However, the accuracy of such SI memory cells in both generations, employing either class A or class AB techniques, is primarily limited by two major errors (Toumazou *et al*.,1993) known as the charge injection errors and the conduction errors.

The charge injection errors are caused by switching mechanisms in the memory switches and may be separated into the channel charge-injection errors and the clock feeedthrough errors (Yuan *et al*., 2001). The conduction errors are caused by an inadequate ratio of the input to the output conductance and a gain-drain capacitive feedback effects (Toumazou *et al*., 1993). Both major errors have been reduced through several techniques such as two-step sampling (S^2I) (Hughes and Moulding, 1993), seamless S^2I (Hughes and Moulding, 1993), and zero-voltage switching (Nairn, 1996) techniques. However, a problem encountered in the S^2I techniques is the slower operation due to the need for two-step (coarse and fine) sampling phases that lead to a reduction in the maximum useful sampling frequency. On the other hand, a problem encountered the zero voltage switching techniques is the typically large differential circuitry that leads to larger complexity and more power consumptions.

In this paper, a low-power low-error single-ended virtually-grounded-drain class AB switched-current memory cell is presented. The proposed circuit is relatively simple based on a basic class AB SI memory cell and a level-shifted grounded-gate amplifier. No large differential circuitry and complicated clocking schemes are required. All charge-injection, clock-feedthrough and conduction errors are reduced. As a design example using 0.5-µm CMOS technology, the power consumption is 120 µW at the bias current of 25 µA and supply voltage of 2V. The optimal sampling frequency is at 45MHz. The SNR, SDR and SFDR are 59.7 dB, 61 dB and 73 dB, respectively. The total harmonic distortion is less than 0.4%. The transmission gain error and the DC offset current error are less than 0.025 and 0.75 µA, respectively. Demonstrations of a forward difference integrator and comparisons to other approaches are also presented.

Analysis of Errors in SI Memory Cells

Charge Injection Errors

Figure 1 shows the basic class A 2nd-generation SI memory cell as a simple example for demonstrating the charge injection errors. Transistors Q_1 and Q_2 form a memory transistor and a current source I_o, respectively. The gate-source capacitance of Q_1 is denoted C_{gs1}. Memory switches S_1, S_2 and S_3 are controlled by a two-phase clock V_{CLK}, i.e. an input phase $\Phi_1[n]$ and an output phase $\Phi_2[n+0.5]$, as shown in Figure 2. The switch S_2 between nodes T_1 and T_2 is formed by transistor Q_3 where C_{OL1} and C_{OL2} are gate-drain and gate-source overlap capacitancesof Q_3, respectively. It can be seen from Figure 2

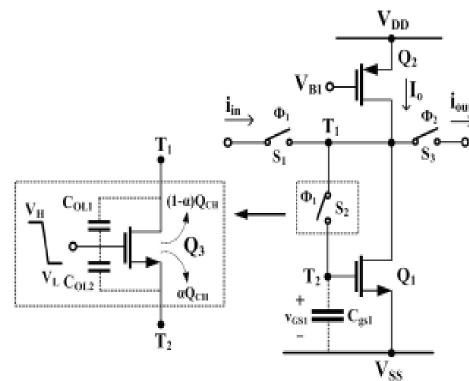

Figure 1. Charg injection errors in the basic class A 2nd- generation SI memory cell

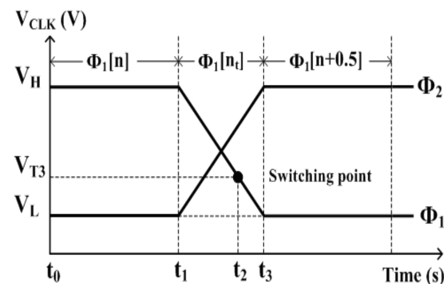

Figure 2. A two-phase clock scheme showing the input phase $\Phi_1[n]$, the additional transition phas $\Phi_1[n_t]$ and the output phase $\Phi_1[n+0.5]$.

that Φ_1 slightly transits from a high voltage level V_H to a low voltage level V_L during time t_1 to t_3 when an additional transition phase may be defined as $\Phi_1[n_t]$. In addition, a threshold voltage V_{T3} of Q_3 determines the switching point of Q_3 at time t_2. The charge injection errors can be demonstrated by the following description.

Firstly, on the input phase $\Phi_1[n_t]$,Q_3 is on and Q_1 is now diode-connected. The input current $i_{in}[n]$ initially flows into node T_1 and a gate-to-source voltage $V_{GS1}[n]$ of Q_1 is subsequently stored on C_{gs1}. The drain current $i_{D1}[n]$ of Q_1 is therefore

$$i_{D1}[n] = I_o + i_{in}[n]=k_1(V_{GS1}[n]-V_{T1})^2 \quad (1)$$

where $k_1 = k'_n W_1/2L_1$, $k'_n = \mu_n C_{ox}$ is a process transconductance parameter, μ_n is an electron mobility, C_{ox} is an oxide capacitance, W_1, L_1 and V_{T1} are the width, the length and the threshold voltage of Q_1, respectively. It follows from (1) that the excess gate voltage of Q_1 is consequently

$$V_{GS1}[n]-V_{T1} = \sqrt{\frac{I_O + i_{in}[n]}{k_1}} \quad (2)$$

Secondly, on the transition phase $\Phi_1[n_t]$, two finite amount of charges q_{CH} and q_{OL} are generated where q_{CH} is a channel charge in the inversion layer underneath the gate existed on the time t_1 to t_2 and q_{OL} is a charge relative to overlap capacitances of Q_3. On the one hand, q_{CH} is approximately given by (Toumazou et al., 1993).

$$q_{CH} = C_{CH}\left(V_H - (1+\frac{\gamma}{3})V_{GS3}[n] - V_{T3}\right) \quad (3)$$

where γ is a back gate parameter, a channel capacitance $C_{CH} = W_3L_3C_{ox}$, W_3, L_3 and V_{T3} are the width, the length and the threshold voltage of Q_3, respectively. A small-signal gate-source voltage $v_{GS3}[n]$ of Q_3 is commonly known as a signal dependent voltage. As the calculations for the exact amount of charges separately injected into the source and drain terminals of the switch transistors are relatively complex (Liang and Harjani, 1998), the amount of charges αq_{CH} and $(1-\alpha)q_{CH}$ are therefore assumed for those injected into nodes T_2 and T_1, respectively, where α is a constant and $0 < \alpha < 1$. The amount of charges $(1-\alpha)q_{CH}$ is absorbed by the input source and has no effect on the sampled-and-held values whilst the amount of charge αq_{CH} is injected into C_{gs1}. On the other hand, the charge q_{OL} is injected into C_{gs1} and can be described throughout the phase $\Phi_1[n_t]$ as

$$q_{OL} = C_{OL2}(V_H-V_L) \quad (4)$$

As a result, a total amount of charge injected into C_{gs1} is $q_T = \alpha q_{CH} + q_{OL}$ and therefore directly affects the stored $v_{GS1}[n]$ by producing an additional charge injection error voltage $\delta v_{GS1}[nt] = q_T/C_{gs1} = (\alpha q_{CH} + q_{OL})/C_{gs1}$. In other words,

$$\delta V_{GS1}[n_t] = \delta v'_{GS1}[n_t] + \delta V''_{GS1} \quad (5)$$

where

$$\delta v'_{GS1}[n_t] = \frac{\alpha C_{CH}(V_H - (1+\frac{\gamma}{3})v_{GS3}[n] - V_{T3})}{C_{gs1}} \quad (6)$$

$$\delta V''_{GS1} = \frac{C_{OL2}(V_H - V_L)}{C_{gs1}} \quad (7)$$

Regarding (6) and (7), Table 1 summarizes corresponding names and types of error voltages due to the charge injection errors based on the dependence of the input current signal (Bengt, 2000).

Thirdly, on the output phase $\Phi_1[n+0.5]$, the resulting drain current $i_{D1}[n+0.5]$ of Q_1 is equal to (Yang *et al*., 1990; Zeng *et al*., 1995)

Table 1. Names and types of error voltages due to charge injection errors.

Error voltages	Names of error voltages	Types of error voltages
$\delta v'_{GS1}[n_t]$	channel charge injection error	a signal-dependent error voltage
$\delta V''_{GS1}$	clock-feedthrough error	a signal-independent error voltage

$$i_{D1}[n+0.5]=k_1(\delta v_{GS1}[n_t]+v_{GS1}[n]-V_{T1})^2 \quad (8)$$

Note that the drain current in (8) on the output phase differs from that in (1) on the input phase due to the charge injection error voltage $\delta v_{GS1}[n_t]$ introduced during $\Phi_1[n_t]$. Substituting the excess gate voltage in (8) with (2) yields

$$i_{D1}[n+0.5]=k_1\left(\delta v_{GS1}[n_t]+\sqrt{\frac{(I_o+i_{in}[n])}{k_1}}\right)^2 \quad (9)$$

Arranging (9) yields the resulting output error current $\delta i_{D1}[n+0.5]=i_{D1}[n+0.5]-i_{D1}[n]$. In other words,

$$\delta i_{D1}[n+0.5]=k_1(\delta v_{GS1}[n_t])^2+2\delta v_{GS1}[n_t]\sqrt{k_1(I_o+i_{in}[n])} \quad (10)$$

The Taylor Series analysis of (10) yields

$$\delta i_{D1}[n+0.5]=\delta i'_{D1}[n+0.5]+\delta i''_{D1}[n+0.5] \quad (11)$$

where

$$\delta i'_{D1}[n+0.5]=k_1(\delta v_{GS1}[n])^2+2\delta v_{GS1}[n]\sqrt{k_1 I_o} \quad (12)$$

$$\delta i''_{D1}[n+0.5]=2\delta v_{GS1}[n]\sqrt{k_1 I_o}\left(\frac{i_{in}[n]/I_o}{2}-\frac{(i_{in}[n]/I_o)^2}{8}\cdots\right) \quad (13)$$

Regarding (12) and (13), Table 2 summarizes resulting output error currents due to the charge injection errors (Bengt, 2000).

Conduction Errors

Figure 3 depicts two identically basic class A 2nd-generation SI memory cells M_A and M_B connected in series as a simple example for demonstrating the conduction errors. With reference to Figure 3, transistors Q_1 and Q_2 form the memory M_A whilst transistors Q_3 and Q_4 form the memory M_B. The gate-source capacitances of Q_1 and Q_3 are C_{gs1} and C_{gs3}, respectively, whilst the gate-drain capacitance of Q_1 is C_{gd1}. The gate-to-source voltages of Q_1 and Q_3 are v_{GS1} and v_{GS3}, respectively.

Table 2. Error currents due to charge injection errors.

Error currents	Resulting output error currents
$\delta i'_{D1}[n+0.5]$	DC Offset current and non-unity gain
$\delta i''_{D1}[n+0.5]$	Non-linear distortion

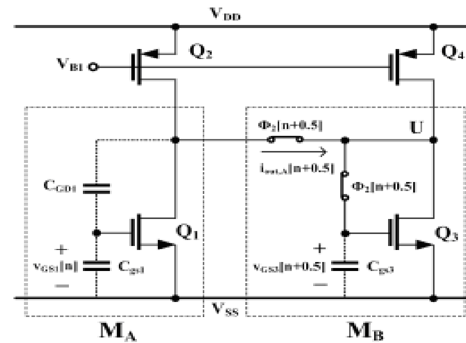

Figure 3. Conduction errors in the cascaded 2nd - generation SI memory cells M_A and M_B.

As shown in Figure 3, the memory M_A is on the output phase $\Phi_2[n+0.5]$ when the gate of Q_1 is held open and delivers an output current $i_{out,A}[n+0.5]$ to memory M_B. Meanwhile M_B is on the input phase $\Phi_1[n+0.5]$ when Q_3 is diode-connected and receives $i_{out,A}[n+0.5]$ or stores the voltage $v_{GS3}[n+0.5]$ on C_{gs3}. Ideally, $i_{out,A}[n+0.5]$ should be completely transferred from M_A to M_B with an unity current transmission gain (G_o). However, G_o is practically less than unity due to the presence of the effective output conductance g_{OM} which is equal to the summation of two conductances g_{OM1} and g_{OM2}, i.e. $g_{OM}=g_{OM1}+g_{OM2}$. The total output conductance g_{OM1} is caused by the channel-length modulation effects at node U, i.e. $g_{OM1}=g_{O1}+g_{O2}+g_{O3}+g_{O4}$ where g_{O1}, g_{O2}, g_{O3} and g_{O4} are the output conductance of Q_1, Q_2, Q_3 and Q_4, respectively. The conductance g_{OM2} is a gate-drain capacitive feedback effect of M_A, i.e. $g_{OM2}=C_{gd1}g_{m1}/(C_{gs1}+C_{gd1})$ where g_{m1} and C_{gd1} are the transconductance and the gate-drain capacitance of Q_1, respectively. Figure4 shows the small-signal equivalent circuit of the cascaded SI memory cells M_A and M_B shown in Figure 3.

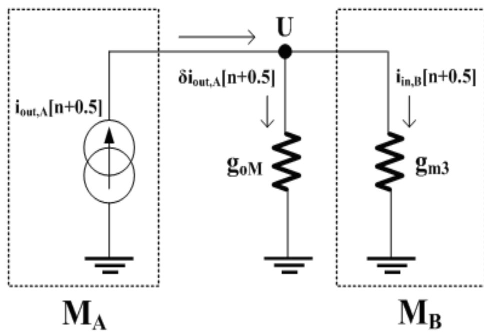

Figure 4. A small-signal equivalent circuit of the cascaded SI memory cells MA and MB shown in Figure 3.

It is seen from Figure 4 that g_{OM} leaks the error current $\delta i_{out,A}[n+0.5] = i_{out,A}[n+0.5] - i_{in,B}[n+0.5]$. As a result, the practical current transmission gain $G_{o1} = i_{in,B}[n+0.5]/i_{out,A}[n+0.5]$ is given by

$$G_{o1} = 1 + \varepsilon_1 \tag{14}$$

$$\varepsilon_1 = -\frac{g_{m3}}{g_{m3} + g_{oM}} \tag{15}$$

where ε_1 is a signal transmission error of the basiccircuit shown in Figure 1. It is evident from (14)and (15) that the conduction error reduces the transmission gain to be less than unity.

Proposed Virtually-Grounded Drain Class AB SI Memory Cell

Circuit Descriptions

Figures 5 and 6 respectively show a block diagram and a circuit configuration of the low-power low- error single-ended virtually- grounded-drain class AB SI memory cell. As shown in Figure-5, the circuit consists of two major components, i.e. a virtually-grounded-drain SI memory M_1 and an offset compensation circuit M_2. The memory M_1 is formed by a basic class AB SI memory cell B_1 (Oliaei and Loumeau, 1998) and a level-shifted grounded-gate amplifier A_1 (Simek an Musil,1998). The memory M_2 is a basic classAB SI memory cell B_2 operating as an offset compensation circuit (Oliaei and Loumeau, 1998). Switches S_1, S_2, S_3, S_4 and S_5 are controlled by a two-phase clock scheme shown in Figure 2. All switches are NMOS transistors and therefore both channel charge injection and clock feeedthrough errors previously described are included.

As shown in Figure 6, B_1 is formed by transistors Q_1 and Q_2 whilst B_2 is formed by transistors Q_3 and Q_4. The amplifier A_1 is formed by transistor Q_5 and two voltage-controlled current sources implemented by transistors Q_6 and Q_7. In terms of small-signal analysis, C_{gsi}, C_{gdi}, g_{mi} and g_{oi} are gate-source capacitance, gate-drain capacitance, transconductance and output conductance of transistors Q_i, respectively, for i = 1 to 7. In term of DC analysis, Table 3 shows bias currents I_{o1}, I_{o2} and I_{o3} where W_i, L_i and V_{Ti} are width, length and threshold voltage of a transistor Q_i, respectively, for i= 1 to 7 and V_{p1},V_{p2},V_{p3} and V_{p4} are DC voltages at the nodes P_1, P_2, P_3 and P_4, respectively.

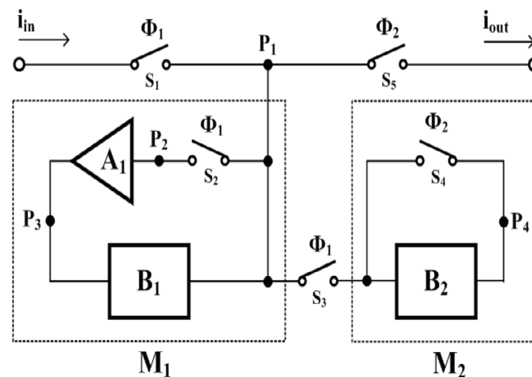

Figure 5. Block diagrams of the proposed single-ended virtually-grounded-drain class AB SI memory cell.

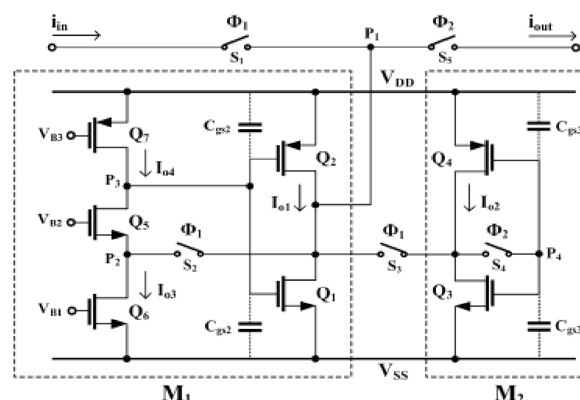

Figure 6. Cicuit diagrams of the proposed single ended virtually-grounded-drain class AB SI memory cell.

Table 3 Bias currents IO1, IO2 , IO3 and IO4.

Bias currents	Formulas
I_{O1}	$k'nW_1(V_{gs1}-V_{T1})^2/2L_1 = k'_pW_2(\lvert V_{gs2}\rvert-\lvert V_{T2}\rvert)^2/2L_2$
I_{O2}	$k'nW_3(V_{gs3}-V_{T3})^2/2L_3 = k'_pW_4(\lvert V_{gs4}\rvert-\lvert V_{T4}\rvert)^2/2L_4$
I_{O3} and I_{O4}	$k'nW_6(V_{gs6}-V_{T6})^2/2L_6 = k'_pW_7(\lvert V_{gs7}\rvert -\lvert V_{T7}\rvert)^2/2L_7$

Reduction in Conduction Errors

On the phase $\Phi_1[n]$, the circuit is configured as shown in Figure 7 where M_1 is a class AB SI memory cell on its sampling phase with a loop formed by A_1 whilst M_2 is on its holding phase. An equivalent circuit at node P_1 is shown in Figure 8. At node P_1, a small-signal input current $i_{in}[n]$ is sampled and develops a small-signal voltage $v_{P1}[n]$, which is subsequently amplified by a voltage gain A of the grounded-gate amplifier. At node P_3, $v_{P3}[n] = A(v_{P1}[n])$ and causes changes in the drain currents of Q_1 and Q_2 by increasing the transconductances g_{m1} and g_{m2} with a factor of A, i.e. Ag_{m1} and Ag_{m2}, as shown in Figure 8. In addition, the effective output conductance g_{OM} at node P_1, resulted from the channel length modulation and the capacitive feedback effects, is $g_{OP1} = g_{O1} + g_{O2} + g_{O3} + g_{O4} + [C_{gd3}g_{m3} / (C_{gd3}+C_{gs3})] + [C_{gd4}g_{m4} / (C_{gd4}+C_{gs4})]$. It can be seen from Figure 8 that Ag_{m1} and Ag_{m2} are much larger than g_{oP1} and therefore the leakage current $\delta i_d[n]$ due to conduction errors is relatively small.

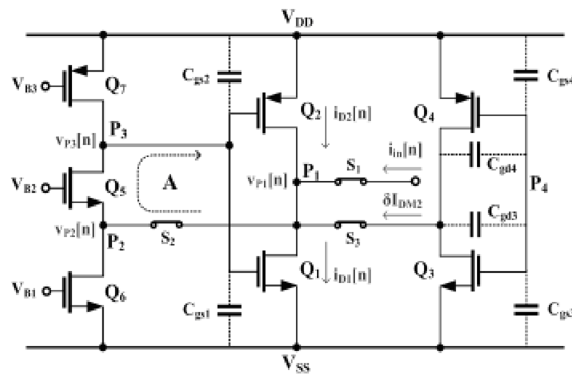

Figure 7. Circuit operations of the proposed SI memory cell shown in Figure 6 on the phase$\Phi_1[n]$.

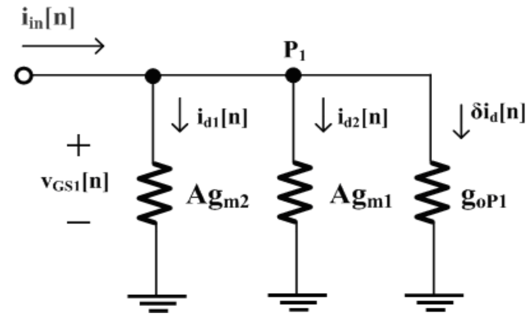

Figure 8. A resulting small-signal circuit dia grams of Figure 6 on the phase $\Phi_1[n]$.

Reduction in Charge Injection Errors

On the phase $\Phi_1[n]$, as shown in Figure 7, the switch S_4 is turned off causing charge-injection errors and therefore M_2 generates an output error current $\delta I_{DM2} = \delta I_{D3} - \delta I_{D4}$ flowing to node P_1 where δI_{D3} and δI_{D4} are error currents in Q_3 and Q_4, respectively, at node P_4, as suggested in (11), (12) and (13). However, as there is no direct presence of input signal i_{in} to the gates of M2, or $i_{in} = 0$ in (13), Table 2 and (12) suggests that δI_{D3} and δI_{D4} become DC offset error currents, i.e.

$$\delta I_{D3} = k_3\left(\delta v_{gs3}\right)^2 + 2\delta v_{gs3}\sqrt{k_3 I_{02}} \quad (16)$$

$$\delta I_{D4} = k_3(\left|\delta v_{gs4}\right|)^2 + 2\left|\delta v_{gs4}\right|\sqrt{k_4 I_{02}} \quad (17)$$

where δV_{gs3} and $|\delta V_{gs4}|$ are error voltages of Q_3 and Q_4 as suggested in (5). When an equilibrium is established, B_1 settles currents $i_{D1}[n]$ and $i_{D2}[n]$ at the drain terminals of Q_1 and Q_2 of value

$$i_{D1}[n] = I_{01} + \left(\frac{Ag_{m1}}{Ag_{m1} + Ag_{m2} + g_{OP1}}\right) i_{in}[n] - \delta I_{D3} \quad (18)$$

$$i_{D2}[n] = I_{01} - \left(\frac{Ag_{m2}}{Ag_{m1} + Ag_{m2} + g_{OP1}}\right) i_{in}[n] + \delta I_{D4} \quad (19)$$

For DC and AC signals, the instantaneous voltage $v'_{P1}[n]$ at the node P_1 is given by

$$V'_{P1}[n] = V_{B2} - V_{GS5} + \left(\frac{i_{in}[n]}{Ag_{m1} + Ag_{m2} + g_{OP1}} \right) \quad (20)$$

On the transition phase $\Phi_1[n_t]$, the switch S_2 is turned off causing charge-injection errors and therefore M_1 generates a channel charge q_{CH} and a charge relative to overlap capacitances q_{OL}. Unlike the charge q_{CH} described in (3), the signal-dependent gate-to-source voltage of the switch S_2 shown in Figure 6, however, is inherently eliminated, i.e. $v_{GS}[n] \approx 0$, as the switch S_2 has been switched at a nearly constant voltage or a virtual ground as described in (20) (Nrain, 1998). Therefore, the charges q_{CH} and q_{OL} produce only a signal-independent error voltage and hence the offset output error currents $\delta I_{D1} \cong \delta I_{D3}$ and $\delta I_{D2} \cong \delta I_{D4}$.

On the phase $\Phi_2[n+0.5]$, the circuit is configured as shown in Figure 9 and its resulting small-signal circuit diagrams is shown in Figure10. It can be seen from Figure 9 that the feedback loop previously formed by A_1 and B_1 is disconnected and therefore the memory M_1 is on the output phase. The memory M_2, on the other hand, is now diode-connected but isolated without the presence of small-signal currents. With reference to Figures 9 and 10, the output currents settling at the drain terminals of the transistors Q_1 and Q_2 are equal to

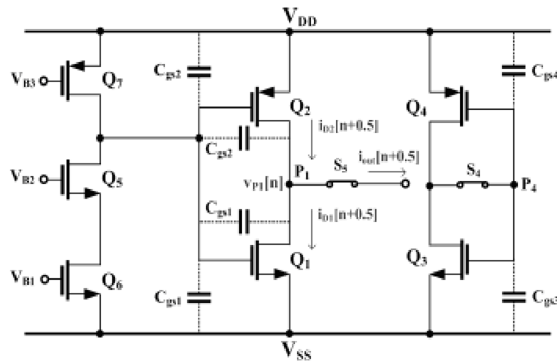

Figure 9. Circuit operations of the proposed SI memory cell shown in Figure 6 on the phase Φ_1[n].

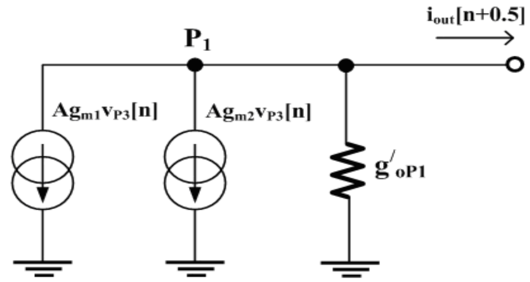

Figure 10. A resulting small-signal circuit diagrams of Figure 9 on the output phase Φ_1[n].

$$i_{D1}[n+0.5] = I_{01} + \left(\frac{Ag_{m1}}{Ag_{m1} + Ag_{m2} + g'_{OP1}} \right) i_{in}[n] - \delta I_{D3} + \delta I_{D1} \quad (21)$$

$$i_{D2}[n+0.5] = I_{01} - \left(\frac{Ag_{m2}}{Ag_{m1} + Ag_{m2} + g'_{OP1}} \right) i_{in}[n] + \delta I_{D4} - \delta I_{D2} \quad (22)$$

where the conductance g'_{oP1} is an effective output conductance at the node P_1 on the phase $\Phi_2[n+0.5]$ and is equal to the summation of g_{oP1} and additional conductance generated by capacitive feedback effects of M_1, i.e $g'_{oP1} = g_{oP1} + C_{gd1}g_{m1}/(C_{gd1} + C_{gs1}) + C_{gd2}g_{m2}/(C_{gd2} + C_{gs2})$. In addition,

$$\delta I_{D1} = k_1 (\delta v_{gs1})^2 + 2\delta v_{gs1} \sqrt{k_1 I_{01}} \quad (23)$$

$$\delta I_{D2} = k_2 (|\delta v_{gs2}|)^2 + 2|\delta v_{gs2}| \sqrt{k_2 I_{01}} \quad (24)$$

As memories M_1 and M_2 are identical, $\delta I_{D1} \cong \delta I_{D3}$ and $\delta I_{D2} \cong \delta I_{D4}$, the output current $i_{out}[n+0.5] = i_{D2}[n+0.5] - i_{D1}[n+0.5]$. In other words

$$i_{out}[n+0.5] = -\left(\frac{Ag_{m1} + Ag_{m2}}{Ag_{m1} + Ag_{m2} + g'_{oP1}} \right) i_{in}[n] \quad (25)$$

where

$$\frac{Ag_{m1} + Ag_{m2}}{Ag_{m1} + Ag_{m2} + g'_{oP1}} \approx 1 - \frac{g'_{oP1}}{A(g_{m1} + g_{m2})} = 1 - \varepsilon_2 \quad (26)$$

where $\varepsilon_2 = g'_{oP1}/A(g_{m1} + g_{m2})$ is a signal transmission error of the proposed circuit. Unlike the errors ε_1 described in (15), the error ε_2 is significantly reduced by the factor of the relatively large gain A. As a result from (25) and (26), the current gain G_{o2} of the output current to the input current is given by

$$G_{o2} = -\frac{i_{out}[n+0.5]}{i_{in}[n]} \approx -1 \qquad (27)$$

A consequent transfer function of the proposed class AB SI memory cell in z-domain $G_{o2}(z) = -I_{out}(z)/I_{in}(z)$ is given by

$$G_{o2} = (Z) = -z^{-\frac{1}{2}} \qquad (28)$$

It can be concluded from (28) that the sampled output current is an inverted half-period delay with a unity gain. In addition, all charge injection, clock-feedthrough and conduction errors are significantly reduced. In conclusion, the proposed SI memory cell utilizes the use of two simple class AB SI memory cell for storing current signals and canceling DC offset errors as well as the grounded-gate amplifier for creating the virtual ground at the drain terminals and hence the name "low-power low-error single-ended virtually-grounded-drain class AB switched-current memory cell"

Performance Analyses

Power Consumption

Power consumption (P_{DC}) is generally described in [W] as $P_{DC} = V_{DC}I_{DC}$ where $V_{DC} = V_{DD} - V_{SS}$ and I_{DC} are the DC supply voltage and the operating DC current, respectively. With reference to Figure 6, the required minimum value of V_{DC} for the class AB SI memories M_1 and M_2 is approximately at $3V_T$ (Worapishet , 2000) assuming the absolute threshold voltages of PMOS and NMOS transistors are equal at V_T. In addition, the current I_{DC} is the summation of operating DC currents shown in Table 3 (Wilcock and Hashimi, 2000). In other words, $I_{DC} = I_{o1} + I_{o2} + I_{o3}$. As a result, the power consumption in the proposed circuit shown in Figure 6 is therefore equal to

$$P_{DC} = \left(I_{o1} + I_{o2} + I_{o3}\right)\left(V_{DD} - V_{ss}\right) \qquad (29)$$

Sampling Frequency

The sampling frequency (F_s) can generally be described in [Hz] through a settling time of a current transfer function in s-domain(Leelavattananon, 1998). With reference to Figure 6, the current transfer function in s-domain is given by

$$\frac{i_{out}(s)}{i_{out}(s)} = \frac{a_o \dfrac{s}{\tau_1}}{s^2 + \dfrac{s}{\tau_1} + \dfrac{1}{\tau_1\tau_2}} \qquad (30)$$

where $$\tau_1 = \frac{C_{gsM1}g_2}{g_{mM1}} \qquad (31)$$

$$\tau_2 = \frac{C_{gs5}g_2 + C_{dsP1}(g_{mM1} + g_2)}{g_{m5}} \qquad (32)$$

$$a_o = \frac{g_{mM1}\left(g_{mM1} + g_2\right)}{g_{m5}} \qquad (33)$$

where τ_1 and τ_2 are time constants, a_o is a DC gain, $g_{mM1} = g_{m1} + g_{m2}$ is a total transconductance of M_1, g_2 is drain-to-source conductance of the switch Q_2, $C_{gsM1} = C_{gs1} + C_{gs2}$ is a total gate-source capacitance of M_1 and C_{dsP1} is a total drain-source capacitances at the node P_1.

It is shown in (30) that the transfer function is a second-order response with two poles consisting τ_1 and τ_2. For purpose of simplicity, such a transfer function can be reduced to a single pole with a single time constant by setting $C_{gs5} = \theta_1 C_{GM1}$ and $C_{dsP1} = \theta_2 C_{GM1}$ and consequently substituting into (31) and (32) where θ_1 and θ_2 are constants. Arranging (31) and (32) yields

$$\tau_2 = \beta\tau_1 \qquad (34)$$

where $\beta = g_{m5}/[(\theta_1 + \theta_2)g_2 g_{mM1} + \theta_2 g_{mM1}]$ is a constant. Upon setting $\beta = 4$ in (34) by adjusting the value of either g_2 or g_{m5} and substituting $\tau_2 = 4\tau_1$

into (30), the transfer function is therefore

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{a_o \frac{s}{\tau_1}}{\left(s + \frac{1}{2\tau_1}\right)} \qquad (35)$$

It is seen from (35) that the resulting transfer function has been reduced to a single pole with a single time constant τ_1. As a proper settling behavior generally requires a minimum settling time of approximately $6\tau_1$ for an accuracy of 0.1%, i.e. the output current reaches 99.9% of the steady state, the maximum F_s of the proposed SI memory cell shown in Figure 6 is therefore $F_s = 1/(6\tau_1)$. In other words,

$$F_s = \frac{g_{mM1}}{6C_{gsM1}g_2} \qquad (36)$$

Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is typically described in [dB] as $10\log(i^2_{signal}/i^2_{noise})$ where i^2_{signal} and i^2_{noise} are a power of a sinusoidal input current and a power of a total output noise current, respectively (Hughes, 2000). On the one hand, i^2_{signal} is typically described by a square of $i_{in,RMS,}$ i.e. $i^2_{signal} = A_m^2/2$. As the amplitude A_m is practicallydetermined by m_iI_o where m_i and I_o are a signal modulation index and the bias current, respectively, i^2_{signal} can be alternatively expressed as

$$i^2_{signal} = \frac{m_i^2 I_0^2}{2} \qquad (37)$$

On the other hand, i^2_{noise} can be described by a total mean square of two dominant noises, i.e.thermal and flicker noises. As the SI memory cells are periodically switched, the flicker noise, however, can be neglected and the total noise is therefore dominated mainly by the thermal noise. With reference to Figure 6, neglecting the thermal noises generated by the switches (Eduard, 1997),the total uncorrelated thermal noises generated by M_1, M_2 and A_1 is $i^2_{noise} = (8/3)m_{th}kTg_{mT}\Delta f$(Fakhfakh,2003) where m_{th} is a process constant, practically ranging from 1 to 2.5, $k = 1.38 \times 10^{-23}$ [J/K] is Boltzmannís constant,T is an absolute temperature in [K], $g_{mT} = \sum_i^7 g_{mi}$ is a total transconductances of all transistors that contribute the thermal noises and $\Delta f = g_{mM1}/4C_{gsM1}$ is a noise bandwidth of the memory M_1. In other words,

$$i^2_{noise} \frac{2m_{th}kT(1+\eta)g^2_{mM1}}{3C_{gsM1}} \qquad (38)$$

where $\eta = (g_{m3} + g_{m4} + g_{m5} + g_{m6} + g_{m7})/(g_{m1} + g_{m2})$ is a constant. As a result from (31) and (32), the SNR of the proposed memory cell can be described as

$$SNR = 10\log\left(\frac{3m_i^2 I_o^2 C_{gsM1}}{3C_{gsM1}}\right) \qquad (39)$$

A Forward Difference SI Integrator

Discrete-time integrators are useful building blocks especially for filters and sigma-delta A/D converters. Several integrators based on SI techniques have been reported including forward difference, backward difference, lossless discrete and bilinear discrete integrators (Helfenstein, 2000). As a particular example, Figures 11 and 12 show the block diagram in z-domain and the circuit configuration, respectively, of the forward difference integrator (Loulou,2003)

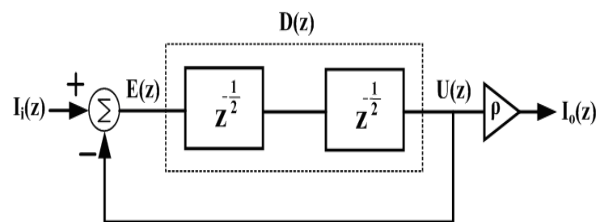

Figure 11. The block diagram in z-domain of the typical forward difference integrator.

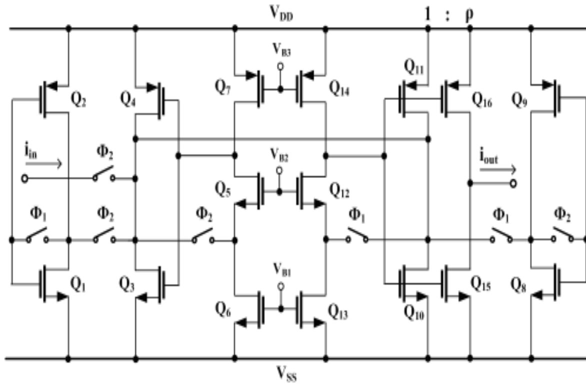

Figure 12. The circuit configuration of the forward difference integrator using the proposed low-power low-error single-ended vir tually-grounded-drain class AB SI memory cells.

using the proposed low-power low-error single ended virtually-grounded-drain class AB SI memory cells. As shown in Figure 11, the integrator is mainly composed of a full-period delay cell with a transfer function D(z) = U(z)/E(z) = z^{-1}. Note that such a delay cell can be implemented by a cascade connection of two SI memory cells with the half period delay transfer function, i.e. $G_o = -z^{-\frac{1}{2}}$ as described in (28). With reference to Figure 12, the resulting transfer function of the integrator is H(z) = $I_o(z)/I_i(z)$. In other words,

$$H(z) = \frac{I_o(z)}{I_i(z)} = \frac{\rho z^{-1}}{1 - z^{-1}} \qquad (40)$$

where ρ is a constant. As shown in Figure 12, transistors Q_1 to Q_7 form the first SI memory cell whilst transistors Q_8 to Q_{14} form the second SI memory cell. In addition, transistors Q_{15} and Q_{16} form a mirrored output with the programmable gain ρ determined through the aspect ratios of Q_{15} and Q_{16}. It can be seen from Figure 12 that the proposed SI memory cell offers an alternative to implement low-power low-error integrator for a variety of applications.

Simulation Results

Performances of the circuits shown in Figure 6 have been simulated through Spice. Transistors are modeled by Alcatel Mietic 0.5-μm CMOS C05MD Technology (AMC) of EUROPRACTICE. Some typical values of the model are summarized in Table 4. As a design example, designed DC and AC parameters used in simulations are summarized in Table 5. In addition, optimally designed aspect ratios (W/L) are summarized in Table 6.

Table 4. Typical values of parameters of the 0.5-μm CMOS technology.

Parameters		Values	
		NMOS	PMOS
Levels		49	49
Threshold voltage (V_T)	V	0.60	-0.61
Minimum length (L_{min})	μm	0.5	0.5
Minimum Width (W_{min})	μm	0.8	0.8
Ambient temperature (T)	K^o	26°	26°

Table 5. Designed parameters used in the simulations, (a) DC values, (b) AC values

	Parameters		Values
(a) DC values	Positive power supply voltage (V_{DD})	V	1
	Negative power supply voltage (V_{SS})	V	-1
	High level clock voltage (V_H)	V	1
	Low level clock voltage (V_L)	V	0
	Bias voltage (V_{B1} and V_{B2})	V	1
	Bias voltage (V_{B3})	V	-1
	Memory bias currents (I_{o1} and I_{o2})	μA	25
	Amplifier bias currents (I_{o3} and I_{o4})	μA	10
(b) AC	Amplitude of the sinusoidal input current (i_{in})	μA	10
	Frequency of the sinusoidal input current (f_{in})	MHz	1

Table 6. Aspect ratios of (a) Memories M_1 and M_2, (b) Amplifier A_1 and (c) Switches of Figure 6.

Transistors / Aspect-ratios	(a) M_1 and M_2		(b) A_1			(b)Switches
	NMOS	PMOS	NMOS		PMOS	NMOS
	Q1,Q3	Q2,Q4	Q5	Q6	Q7	
W/L μm/μm	3.75/1	7.25/0.5	5/0.5	1/0.5	2.5/0.5	0.8/0.5

Table 7 compares values of performances of the circuit shown in Figure 6 between the analysis and simulation. Figure 13 shows the settling behavior of the output current I_{out} (µA) and the rectangular pulse of input current I_{in} with the amplitude and the pulse width of 25 µA and 6 ns, respectively. It is seen from Figure 13 that I_{out} exhibits a settlingtime at 0.1 % error of 3.65 ns and therefore the possible maximum F_s is approximately at 45.6 MHz. Figure 14 depicts plots of a current transfer curve of the input current i_{in} (µA) versus the output current i_{out} (µA). As shown in Figure 14, the transfer curve exhibits a relatively linear characteristic, particularly at i_{in} below 50 µA. In addition, the maximum output signal swing is approximately 75 µA which is larger than the operating bias current Io of 25 µA.

Table 7. Values of performances of Figure 6 from (a) analysis and (b) simulation.

Performances	Equations	(a) Analysis	(b) Simulation
P_{DC}	(29)	120 µ	126 µW
Maximum F_s	(30)	51.2 MHz	45.6 MHz
SNR at F_s = 45 MHz, f_{in} = 4.5 MHz	(32)	60.3 dB	56.2 dB
at F_s = 10 MHz, f_{in} = 1 MHz	(32)	60.3 dB	59.7dB

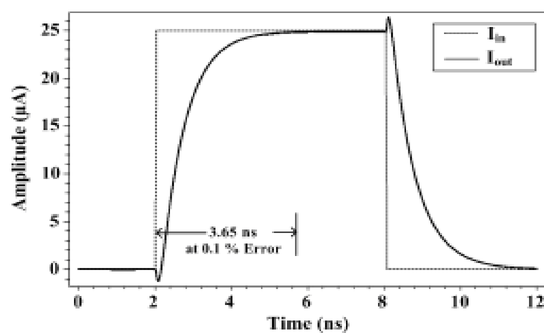

Figure 13. Settling behaviors of the output current I_{out} of Figure 6 showing the settling time at 0.1% error of approximately 3.65 ns.

Figure 15 depicts plots of a DC offset output current error (µA) versus the input current i_{in} (µA) where the dotted lines indicate the ideal values as well as the solid lines indicate the Spice analysis. As shown in Figure 16, the DC offset current errors are less than 0.75 µA over the input current in the region of 0 of 25 µA. Figure 16 illustrates waveforms of the sampled output current i_{out} (inverted) and the sinusoidal input current iin at F_s = 10 MHz and f_{in} = 1 MHz, respectively. It is clearly seen from Figure 16 that i_{out} readily follows the expected function, i.e. a half-period delay, with a unity current gain.

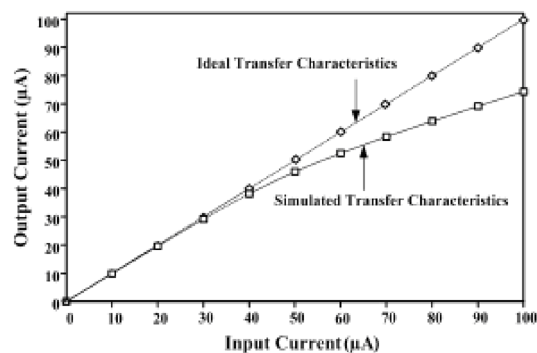

Figure 14. Plots of the current transfer curve of the output current I_{out} in (µA) versus the input current I_{in} (µA) of Figure 6.

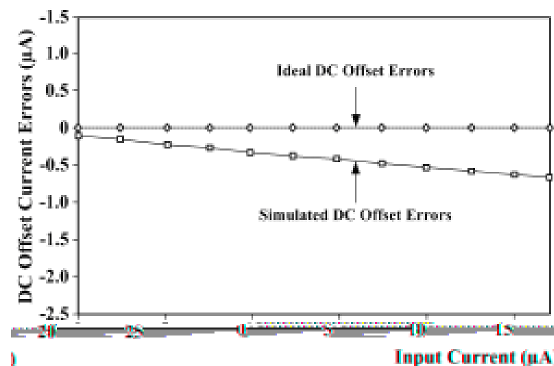

Figure 15. Plots of the DC offset current errors (µA) versus the input current I_{in} (µA) of Figure 6.

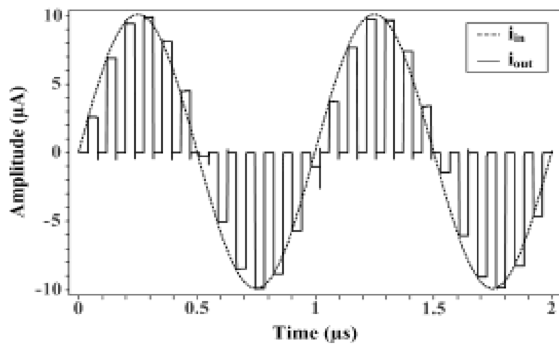

Figure 16. The waveforms of the sampled output current i_{out} (inverted) and the sinusoidal input current iin at F_s = 10 MHz and f_{in} = 1 MHz, respectively.

Figure 17 shows the power spectrum levels (dB) of the fundamental frequency at 1MHz, the harmonics and the spurious tones of the sampled output current iout previously depicted in Figure 16 using a 2048-point Fast Fourier Transform (FFT). As shown in Figure 17, the distortions are due mainly to the presence of the second harmonics and the largest spurious tone. Consequently, a signal-to-distortion ratio (SDR) defined as the difference of the fundamental frequency and the highest harmonic (Renyuan and Chin-Long , 1998) is 61 dB. In addition, the spurious free dynamic range (SFDR) defined as the difference of the fundamental frequency and the largest spurious tone (Jacob, 2002) is 73 dB.Figure 18 depicts the input and output current waveforms with 90° degree phase difference of the forward difference integrator shown in Figure 11.

Comparisons

Table 8 particularly compares the simulation results between this paper and other proposed SI memory cells employing either (a) class A or (b) class AB techniques. In terms of performances,this paper offers a low power consumption of 120 µW at the bias current of 25 µA and the supply voltage of 2V using 0.5-µm CMOS technology. The minimum transmission and DC offset errors are less than 0.025 and 0.75 µA, respectively. With the optimal design of the aspect ratios, the optimal sampling frequency is at 45.6 MHz. The SNR, SDR and SFDR are 59.7 dB, 61 dB and 73 dB,respectively. The THD is less than 0.4%.

In terms of circuit design, the proposed technique, i.e. the use of a simple class AB SI memory cell and a grounded-gate amplifier, reduces both signal-dependent and signal-independent errors caused by charge-injection and conduction errors. In addition, no external capacitors, complicated 3or 4 clock phases and large differential circuitry are required. This work therefore offers not only much better performance compared to those SI memory cells using either class A or class AB techniques but also a potential alternative to a low-power low error SI memory cell with the simple single-ended configuration and two-phase clock scheme.

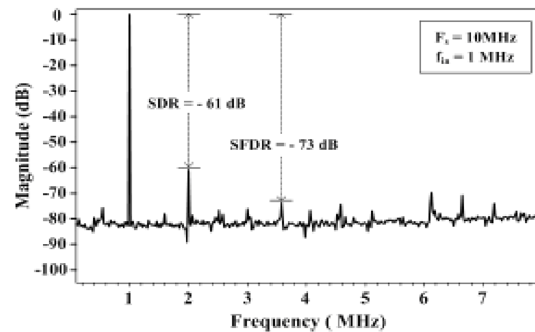

Figure 17. Power spectrum through 2048-point FFT of the sampled output current waveform previously depicted in Figure 16 demonstrating SDR = 61 dB and SFDR = 71 dB.

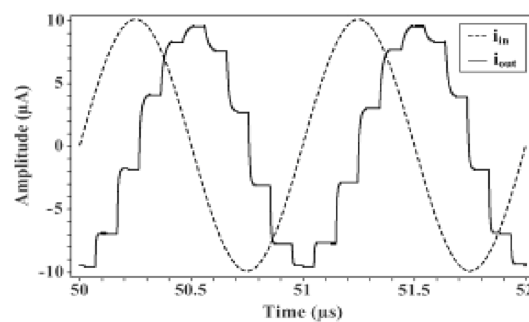

Figure 18. The input and output current wave forms with 90° degree phase difference of the forward difference integrator depicted in Figure13.

Table 8. Comparisons of simulation results between this paper and other proposed SI memory cells using (a) class A techniques and (b) class AB techniques, √ = Yes, X = No.

Performance \ References			Switched-current memory cells										
			(a) Class A techniques				(b) Class AB techniques						
			(Hughes and Moulding, 1997)	(Leelavattanan and et al., 1998)	(Balachandran and Allen, 1999)	(Rout and Lee, 2000)	(Balachandran and Allen 2001)	(Igor , 1999)	(Srowik and Schuffny, 1999)	(Grech,2000)	(Sitdhikorn et al., 2001)	(Loulou et al., 2003)	This paper
Minimum Length of CMOS Technology (μm)			0.5	0.8	0.8	0.25	0.35	-	-	-	0.35	0.35	**0.5**
performances	I_o	μA	-	100	100	400	600	1	6.8	5	25	90	**25**
	i_{in} (Maximum)	μA	-	5	75	100	590	18	60	50	10	300	**75**
	V_{DC}	V	3.3	3.3	3.3	1	3.3	1	2.5	1.4	1.6	3.3	**2**
	t_s (0.1%)	ns	-	-	5.5	4.7	< 300	-	-	-	-	-	**3.65**
	F_s (Maximum)	MHz	80	0.02	-	100	13	2	-	0.2	100	16	**45.6**
	SNR	dB	-	-	-	-	60	-	-	-	69.6	-	**59.7**
	SDR	dB	-	-	-	-	-	-	-	-	-	-	**61**
	SFDR	dB	-	-	-	-	-	-	-	-	-	-	**73**
	THD.	%	-	0.03%	-	-	-	-	-	-	-	-	**< 0.4**
	P_{DC}	μW	-	-	1000	1640	-	-	22.6	-	-	-	**120**
	Transmission error	%	0.001	0.001	< 0.1	-	< 0.4	4.3	-	0.05	< 0.2	-	**< 0.025**
	DC offset error	μA	-	2.4	-	-	-	-	-	-	-	-	**< 0.75**
	Number of clock phase	-	3	3	3	1	4	3	2	3	3	4	**2**
others	Using internal capacitances		√	√	√	√	X	X	√	√	√	√	√
	Using the single-ended configuration		X	√	X	X	X	√	√	X	X	X	√
	Reduction in signal dependent errors		√	X	√	√	√	X	X	√	√	√	√
	Reduction in signal independent errors		√	√	√	√	√	X	X	√	√	√	√

Conclusions

A low-power low-error single-ended virtually-grounded-drain class AB switched-current memory cell has been presented. The proposed circuit is relatively simple based on a basic class AB SI memory cell and a level-shifted grounded-gate amplifier. No large differential circuitry and complicated clocking schemes are required. All charge-injection,clock-feedthrough and conduction errors are reduced. As a design example using 0.5- μm CMOS technology, the power consumption is 120 μW at the bias current of 25 μA and supply voltage of 2V. The optimalsampling frequency is at 45MHz.The The SNR, SDR and SFDR are 59.7 dB, 61 dB and73 dB,respectively.The total harmonic distortion is less than 0.4%. The transmission gain and the DC offset current errors are less than 0.025 and 0.75 µA,respectively. Demonstrations of a forward difference integrator and comparisons to other approaches are also presented.

Acknowledgements

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